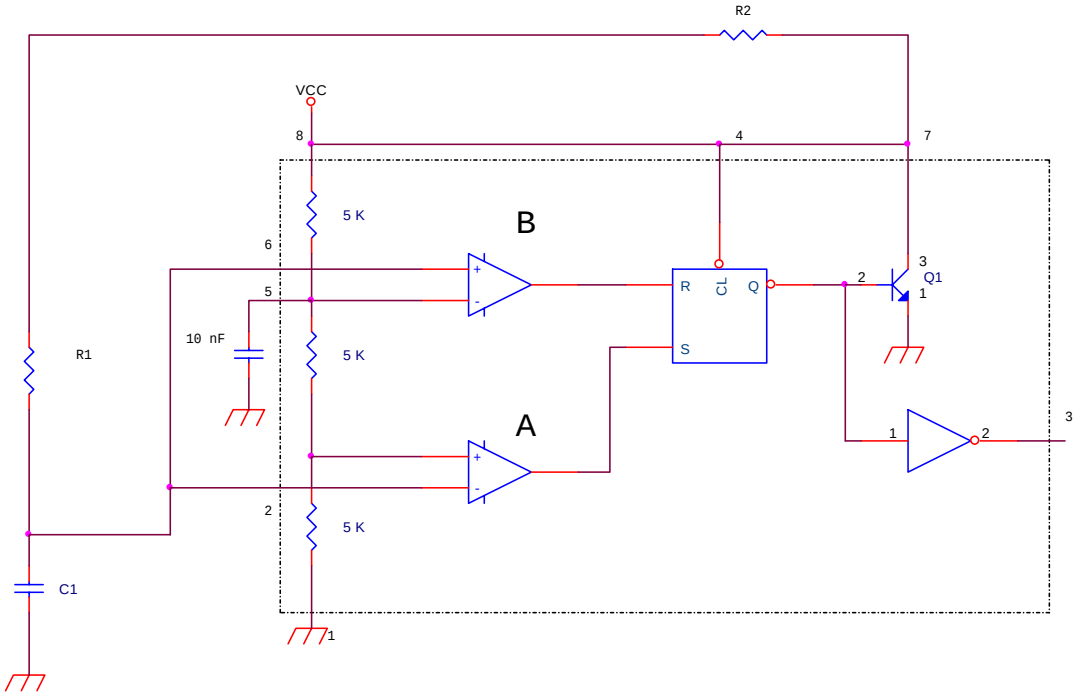
Generatore di clock mediante NE 555

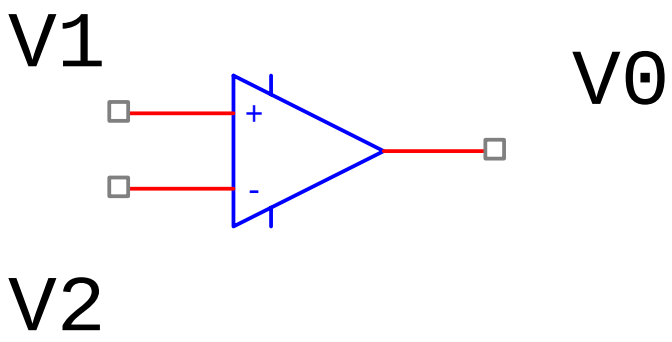
Consideriamo la seguente figura



L'integrato NE555 è rappresentato dalla parte racchiusa dalla linea tratteggiata. I numeri presenti in prossimità di tale linea individuano i pin dell'integrato. Si nota, all'interno dell'integrato, un latch di tipo SR. Un latch di tipo SR è un circuito sequenziale con due ingressi denominati S ed R e due uscite Q e $\overline{Q}$ che soddisfano la seguente tabella

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	X	X

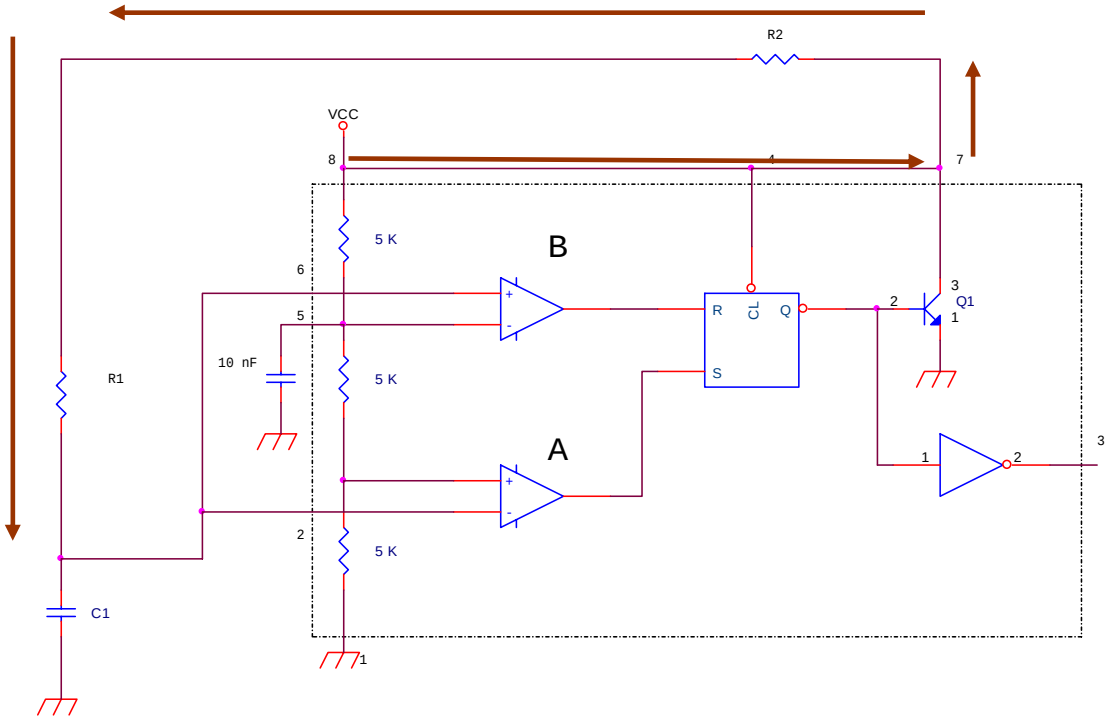
La prima combinazione degli ingressi fa in modo che le uscite permangano ai valori che avevano precedentemente. L'ultima combinazione non è utilizzata. Come si può notare dalla figura, i segnali S ed R sono ricavati dalle uscite di due comparatori (individuati dai due simboli triangolari). Inoltre il latch contenuto nell'integrato presenta la sola uscita negata $\overline{Q}$. Un comparatore di tensione è un dispositivo che presenta un'uscita e due morsetti individuati rispettivamente con un + ed un –



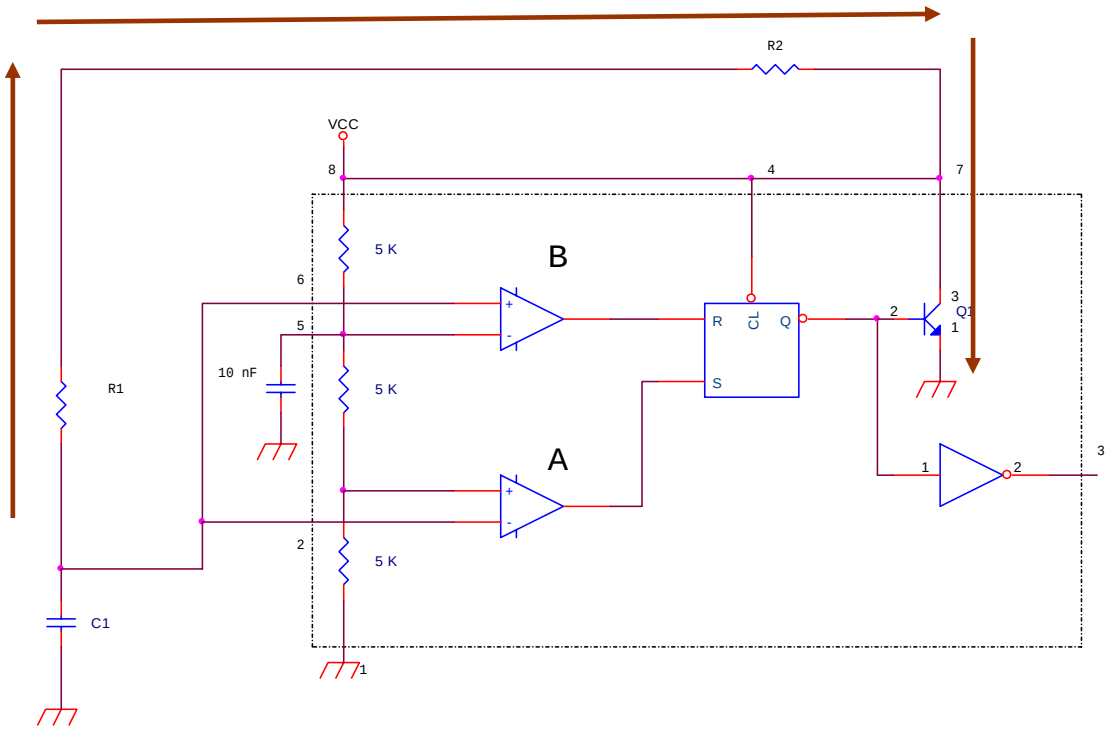
Questo dispositivo confronta le due tensioni V_1 e V_2 presenti agli ingressi dell'operazionale. Se $V_1 > V_2$, l'uscita si porta a livello logico alto, se $V_1 < V_2$ l'uscita si porta a livello logico basso. La condizione $V_1 = V_2$ seppur logicamente possibile, non può, in realtà verificarsi in quanto, essendo il comparatore estremamente sensibile, basta una differenza infinitesima fra i due segnali a far scattare il comparatore. All'interno del NE555 vi è un partitore resistivo costituito da tre resistenze in serie da 5 kohm. Ne deriva che al morsetto - del comparatore indicato con la lettera B nello schema arriva una tensione pari a $\frac{2}{3}V_{CC}$ mentre al morsetto + del comparatore indicato con la lettera A giunge la tensione di $\frac{1}{3}V_{CC}$. I componenti che, nella figura, appaiono all'esterno della linea tratteggiata non fanno parte dell'integrato e sono aggiunti per fare in modo che esso si comporti come un circuito astabile. *Un circuito astabile è un circuito che non presenta ingresso e la cui uscita oscilla. Il condensatore da 10 nF collegato al piedino 5 ha lo scopo di mantenere stabile la tensione fornita dal partitore resistivo.*

All'accensione il condensatore C_1 alla sinistra del circuito è scarico per cui al morsetto + del comparatore B giunge una tensione nulla. Poiché al morsetto –

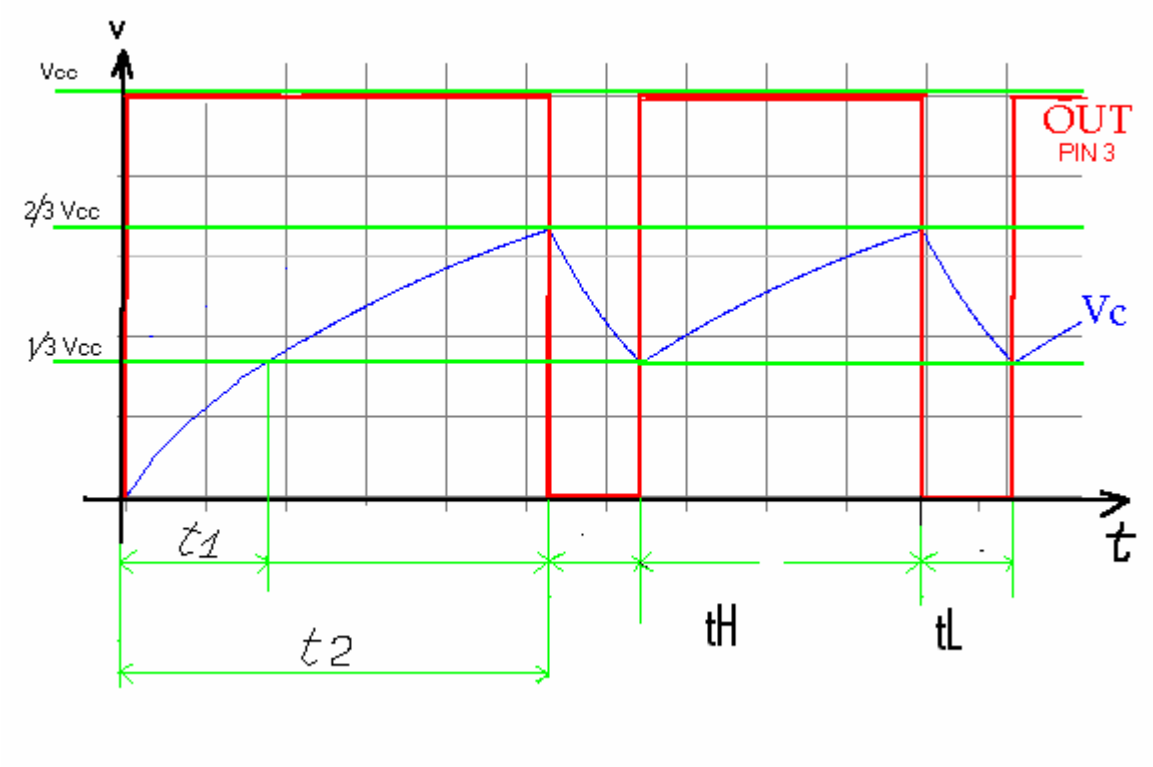
giunge una tensione superiore, l'uscita del comparatore è pari a 0. Inversamente per il comparatore inferiore, abbiamo al morsetto – una tensione nulla per cui questa è inferiore a quella al morsetto + e l'uscita è a livello logico alto. Si ha che S = 1 ed R = 0, il latch è settato per cui Q = 1 e $\overline{Q}$ = 0. Ma quest'ultimo comanda la base del BJT che risulterà, pertanto, in interdizione. Poiché un transistor in interdizione si comporta da circuito aperto, il condensatore C_1 risulta collegato, attraverso le resistenze R_1 ed R_2 alla tensione di alimentazione V_{CC} per cui può caricarsi



La tensione ai capi del condensatore aumenta. Ad un certo istante essa raggiungerà il valore $\frac{V_{CC}}{3}$, per cui l'uscita del comparatore A passerà dal valore logico 1 al valore logico zero. Per quanto riguarda il comparatore B, a questo punto la tensione al morsetto + è ancora inferiore a quella presente al morsetto – per cui la sua uscita permane al livello logico zero. Gli ingressi del latch sono allora S = 0 ed R = 0. dalla tabella precedente si vede che le uscite permangono al livello precedente per cui il BJT resta interdetto e il condensatore continua a caricarsi. Quando la sua tensione giunge al valore $\frac{2V_{CC}}{3}$, l'uscita del comparatore B passa al valore logico uno. Gli ingressi del latch diventano S = 0 ed R = 1 e le uscite commutano a Q = 0 e $\overline{\overline{Q}}$=1. il BJT va in saturazione trasformandosi in un corto circuito. Da questo momento il condensatore C, attraverso la resistenza R2 ed il BJT viene posto a massa e, quindi si scarica



Quando la tensione del condensatore scende di nuovo al di sotto del valore $\frac{V_{CC}}{3}$ si ha di nuovo la condizione S =1 ed R = 0, per cui l'uscita $\bar{\bar{Q}}$ va di nuovo a zero, conseguentemente il BJT va di nuovo in interdizione ed il condensatore risulta di nuovo collegato alla VCC e si può ricaricare di nuovo. Da questo momento la tensione del condensatore oscillerà fra $\frac{V_{CC}}{3}$ e $\frac{2V_{CC}}{3}$. Si osservi che, quando il condensatore sta caricando si ha $\bar{\bar{Q}} = 0$ per cui l'uscita dell'integrato, essendo negata sarà a livello logico uno. Invece, quando il condensatore sta scaricando, si ha $\bar{\bar{Q}} = 1$ per cui l'uscita dell'integrato va a zero.



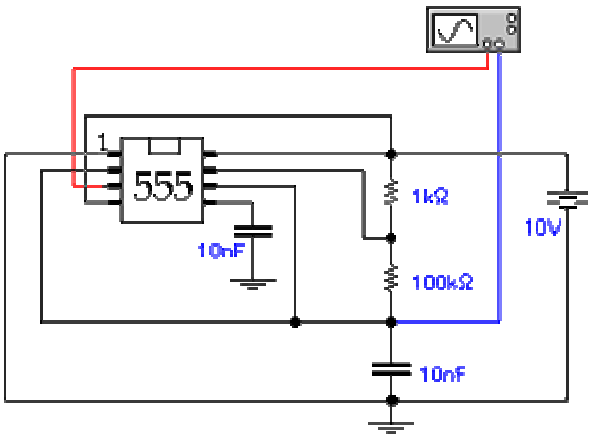
Otteniamo dunque, un'onda quadra. Nella figura la linea blu indica l'andamento della tensione ai capi del condensatore e la linea rossa rappresenta l'andamento dell'uscita Per calcolare il periodo e il duty cycle della stessa dovremmo effettuare alcuni calcoli, ma possiamo già osservare che il tempo t_H durante il quale l'uscita è alta dipende dal tempo che il condensatore mette a caricarsi, per cui è proporzionale alla tau di carica, che a sua volta è pari a $\tau_C = C(R_1 + R_2)$. Analogamente il tempo t_L durante il quale l'onda rimane a livello basso sarà proporzionale al tempo di scarica, a sua volta proporzionale alla tau di scarica $\tau_S = C(R_2)$, ne deriva che t_H deve necessariamente essere superiore a t_L per cui

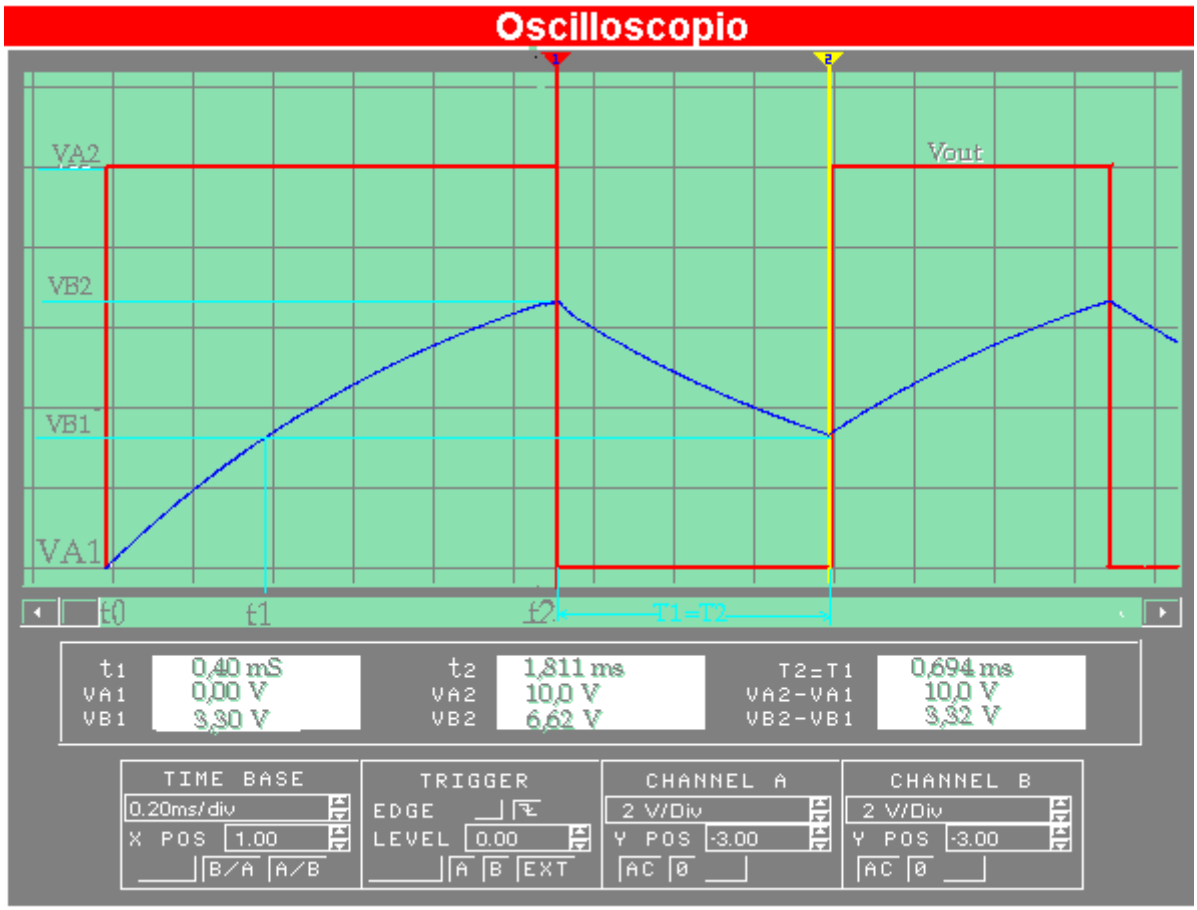
$$\frac{t_H}{T} = \frac{t_H}{t_H + t_L} > \frac{1}{2}$$

cioè il duty cycle è

$$D\% = \frac{t_H}{T}100 = \frac{t_H}{t_H + t_L}100 > 50\%$$

Ora dobbiamo trovare una formula di progetto che leghi i valori delle capacità e resistenze inserite nel circuito al valore di frequenza che si vuole ottenere.

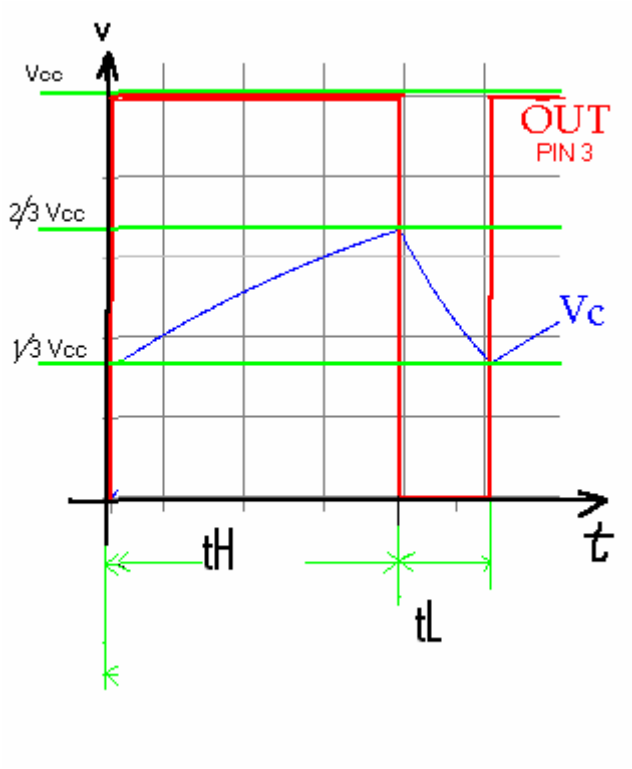




L'equazione differenziale che regge il fenomeno della carica e scarica in un circuito RC ha per soluzione generale la seguente espressione

$$v_C(t) = Ae^{-\frac{t}{\tau}} + B$$

dove A e B sono due costanti che dipendono dalle condizioni iniziali. Cerchiamo, allora di calcolare il tempo t_H e supponiamo di fissare l'istante iniziale t = 0, proprio quando il condensatore inizia a caricarsi.



per t = 0 si ha $v_C(t) = \frac{V_{CC}}{3}$, quindi

$$v_C(0) = Ae^{-\frac{0}{\tau}} + B = Ae^0 + B = A*1 + B = A + B = \frac{V_{CC}}{3}$$

Ora notiamo che, se il condensatore fosse lasciato libero di caricarsi, in un tempo infinito avremmo

$$t \to \infty \Rightarrow v_C(t) \to V_{CC}$$

$$\lim_{t \to \infty} \quad v_C(t) = Ae^{-\infty} + B = A*0 + B = B = V_{CC}$$

abbiamo allora che

$$\begin{cases} A+B=\dfrac{V_{CC}}{3} \Rightarrow A=\dfrac{V_{CC}}{3}-B=\dfrac{V_{CC}}{3}-V_{CC}=-\dfrac{2V_{CC}}{3} \\ B=V_{CC} \end{cases}$$

la legge che regola nel nostro caso, la carica e scarica di un condensatore è allora

$$v_C(t)=-\frac{2V_{CC}}{3}e^{-\frac{t}{\tau_C}}+V_{CC}$$

dal grafico si vede che per t = t_H, $v_C(t)=\frac{2V_{CC}}{3}$ quindi

$$v_C(t)=-\frac{2V_{CC}}{3}e^{-\frac{t_H}{\tau_C}}+V_{CC}=\frac{2V_{CC}}{3}$$

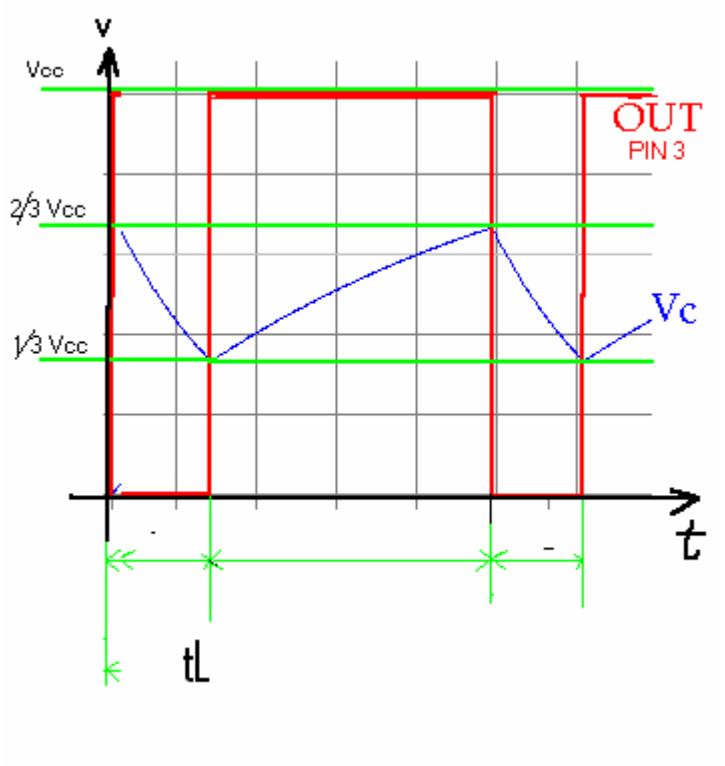
$$-\frac{2}{3}e^{-\frac{t_H}{\tau_C}}+1=\frac{2}{3}\Rightarrow -\frac{2}{3}e^{-\frac{t_H}{\tau_C}}=\frac{2}{3}-1\Rightarrow -\frac{2}{3}e^{-\frac{t_H}{\tau_C}}=-\frac{1}{3}\Rightarrow$$

$$e^{-\frac{t_H}{\tau_C}}=\frac{1}{2}\Rightarrow \ln e^{-\frac{t_H}{\tau_C}}=\ln\frac{1}{2}\Rightarrow$$

$$\ln e^{-\frac{t_H}{\tau_C}}=\ln\frac{1}{2}\Rightarrow -\frac{t_H}{\tau_C}=-\ln 2\Rightarrow t_H=\tau_C\ln 2\Rightarrow$$

$$t_H\approx 0.7(R_1+R_2)C$$

ripetiamo lo stesso procedimento per la scarica, ponendo t = 0 all'istante in cui comincia a scaricarsi il condensatore



$$v_C(t) = Ae^{-\frac{t}{\tau_S}} + B$$

per t = 0 si ha $v_C(t) = \frac{2*V_{CC}}{3}$,

$$v_C(0) = Ae^{-\frac{0}{\tau}} + B = Ae^0 + B = A*1 + B = A + B = \frac{2*V_{CC}}{3}$$

Ora notiamo che, se il condensatore fosse lasciato libero di scaricarsi, in un tempo infinito avremmo

$$t \to \infty \Rightarrow v_C(t) \to 0$$

$$\lim_{t \to \infty} v_C(t) = Ae^{-\infty} + B = A*0 + B = B = 0 \Rightarrow$$

$$A = \frac{2V_{CC}}{3} \Rightarrow v_C(t) = \frac{2V_{cc}}{3} e^{-\frac{t}{\tau_S}}$$

dal grafico si vede che per t = t_L , $v_C(t) = \frac{V_{CC}}{3}$ quindi

$$v_C(t) = \frac{2V_{CC}}{3} e^{-\frac{t_L}{\tau_S}} = \frac{V_{CC}}{3}$$

$$e^{-\frac{t_L}{\tau_S}} = \frac{1}{2} \Rightarrow \ln e^{-\frac{t_L}{\tau_S}} = \ln \frac{1}{2} \Rightarrow$$

$$-\frac{t_L}{\tau_S} = -\ln 2 \Rightarrow t_L = \tau_S \ln 2 \Rightarrow$$

$$t_L \approx 0.7(R_2)C$$

Il periodo dell'onda quadra è allora

$$T = t_H + t_L = 0.7(R_1 + R_2)C + 0.7R_2C = 0.7(2R_2 + R_1)$$

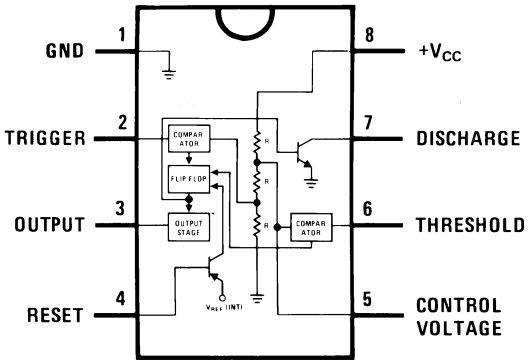
$$f = \frac{1}{0.7(R_1 + 2R_2)C}$$

Precision Timer

NE555

Connection Diagram

SO-8 NE555M



DIP-8 NE555N

FUNCTION TABLE

RESET	TRIGGER VOLTAGE	THRESHOLD VOLTAGE	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3V_{DD}	High	High	Off
High	>1/3V_{DD}	>2/3V_{DD}	Low	On
High	>1/3V_{DD}	<2/3V_{DD}	As previously established	

General Description

The NE555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ OUTPUT LOW		3	6	mA
	V_{CC} = 15V, R_L = ∞ OUTPUT LOW		10	15	
Note 4	Vcc=5V,No load OUTPUT HIGH		2	5	
Timing Error, Monostable					
Initial Accuracy			1	3	%
Drift with Temperature	R_A = 1k to 100kΩ,		50		ppm/°C
	C = 0.1µF, (Note 5)				
Accuracy over Temperature			1.5		%
Drift with Supply			0.1	0.5	%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ,		150		ppm/°C
	C = 0.1µF, (Note 5)				
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.5	5	5.6	V
	V_{CC} = 5V	1.1	1.67	2.2	V
Trigger Current	Trigger at 0V		0.5	2	uA
Reset Voltage		0.3	0.7	1	V
Reset Current	Reset at Vcc		0.1	0.4	mA
Threshold Current	(Note 6)		30	250	nA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			20	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA		0.15	0.4	V
	I_{SINK} = 5mA		0.1	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100	300	ns
Fall Time of Output			100	300	ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance 170°C/W (S0-8), junction to ambient.

Note 4: Supply current when output high typically 9mA and MAX. is 13mA at Vcc=15V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

RECOMMENDED OPERATING

	MIN	MAX.	UNIT
Supply voltage ,Vcc	**4.5**	**16**	**V**
Input voltage (control,reset,threshold, and trigger)		**Vcc**	
Output current		**±200**	**mA**
Operating free-air temperature, T_A	**0**	**70**	**°C**

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

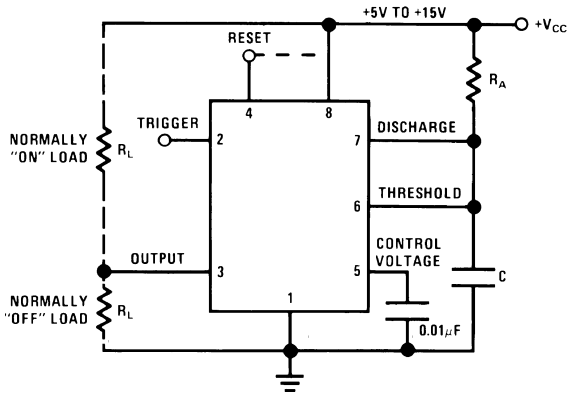
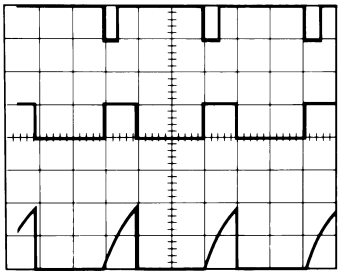


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

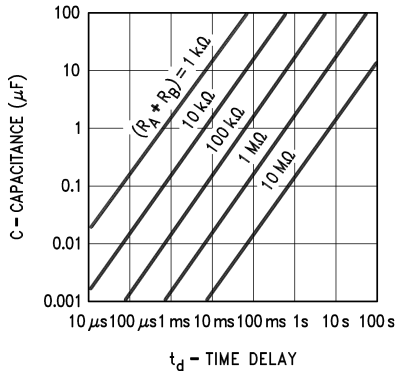


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

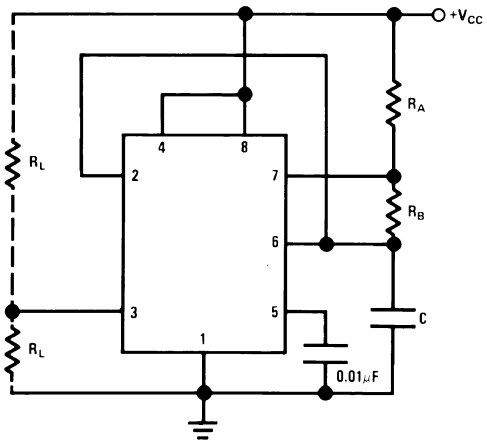
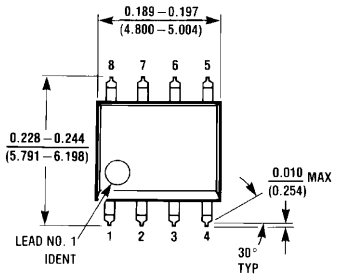


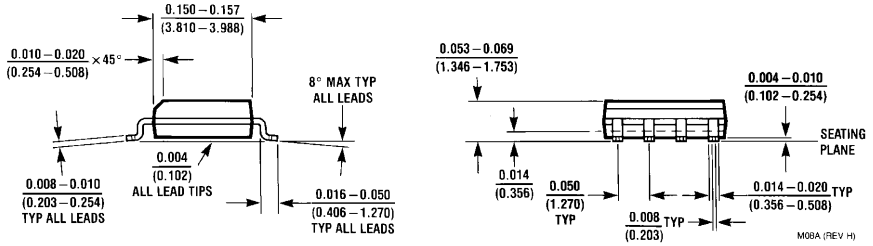
FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

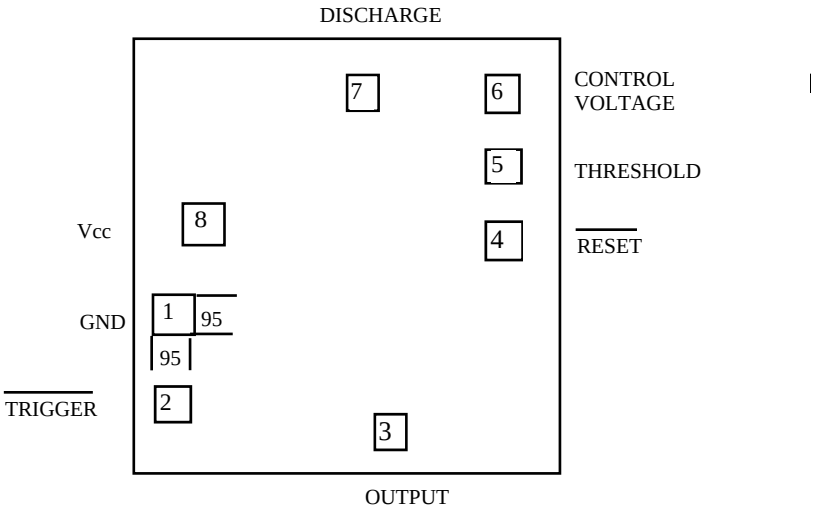
Physical Dimensions inches (millimeters) unless otherwise noted

NE555M





Pad locatin



Chip Size: 1.02x 1.07 mm

Pad N	Pad Name	Coordinates mkm	
		X	Y
1	GND	95	313
2	$\overline{\text{TRIGGER}}$	115	126
3	OUTPUT	590	126
4	$\overline{\text{RESET}}$	810	451
5	THRESHOLD	810	635
6	CONTROL VOLTAGE	780	829
7	DISCHARGE	420	893
8	Vcc	125	492

DATA SHEET

NE/SA/SE555/SE555C
Timer

Product data
Supersedes data of 1994 Aug 31

2003 Feb 14

Philips
Semiconductors

PHILIPS

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

FEATURES

- Turn-off time less than 2 μs
- Max. operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

PIN CONFIGURATION

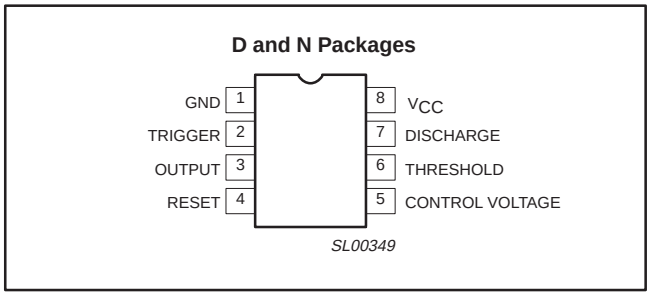


Figure 1. Pin configuration

BLOCK DIAGRAM

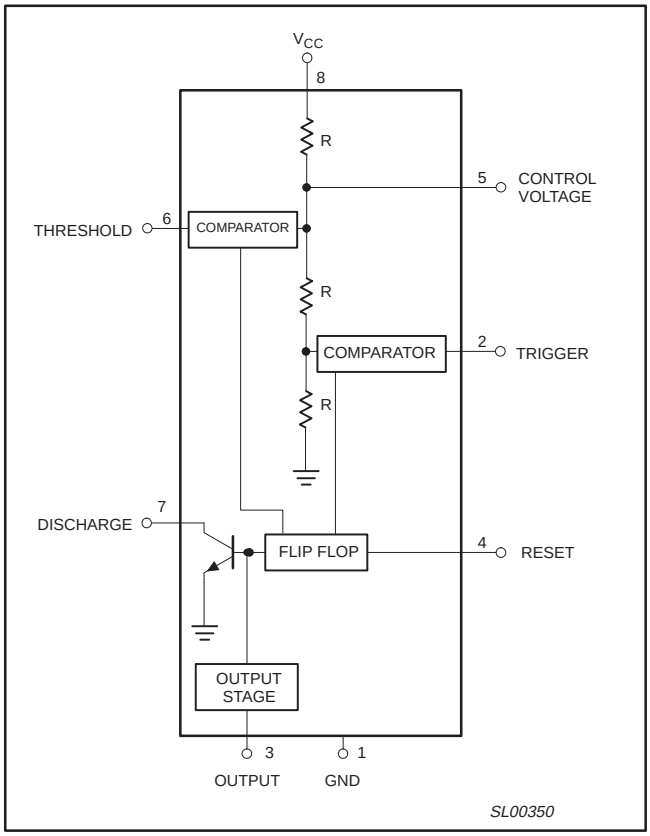


Figure 2. Block Diagram

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70 °C	NE555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE555N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–40 °C to +85 °C	SA555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +85 °C	SA555N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE555CN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE555N	SOT97-1

EQUIVALENT SCHEMATIC

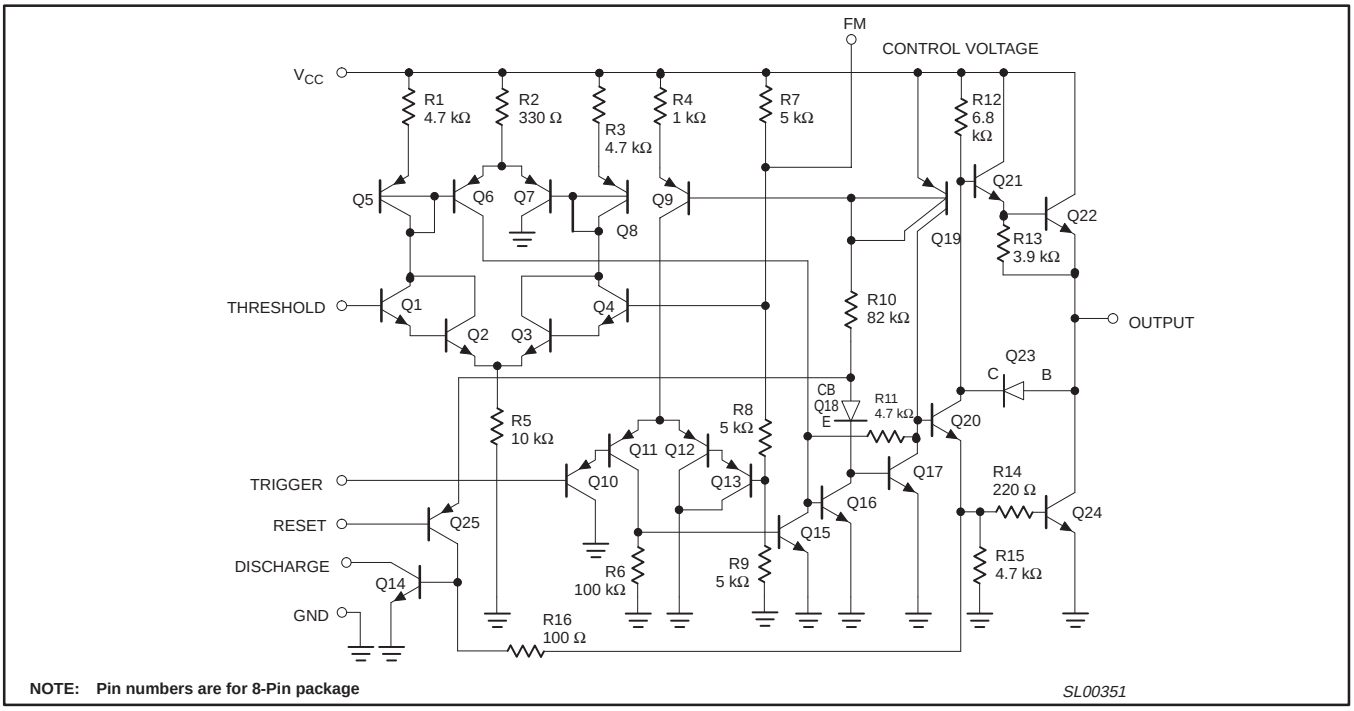


Figure 3. Equivalent schematic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE555 NE555, SE555C, SA555	 +18 +16	 V V
P_D	Maximum allowable power dissipation[1]	600	mW
T_{amb}	Operating ambient temperature range NE555 SA555 SE555, SE555C	 0 to +70 –40 to +85 –55 to +125	 °C °C °C
T_{stg}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	+230	°C

NOTE:

1. The junction temperature must be kept below 125 °C for the D package and below 150°C for the N package.
   At ambient temperatures above 25 °C, where this limit would be derated by the following factors:
   D package 160 °C/W
   N package 100 °C/W

DC AND AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = +5 V to +15 V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SA555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC} = 5 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞		3 10	5 12		3 10	6 15	mA mA
t_M $\Delta t_M/\Delta T$ $\Delta t_M/\Delta V_S$	Timing error (monostable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A = 2 kΩ to 100 kΩ C=0.1 μF		 0.5 30 0.05	 2.0 100 0.2		 1.0 50 0.1	 3.0 150 0.5	 % ppm/°C %/V
t_A $\Delta t_A/\Delta T$ $\Delta t_A/\Delta V_S$	Timing error (astable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A, R_B = 1 kΩ to 100 kΩ C = 0.1 μF V_{CC} = 15 V		 4 0.15	 6 500 0.6		 5 0.3	 13 500 1	 % ppm/°C %/V
V_C	Control voltage level	V_{CC} = 15 V V_{CC} = 5 V	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
V_{TH}	Threshold voltage	V_{CC} = 15 V V_{CC} = 5 V	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC} = 15 V V_{CC} = 5 V	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
I_{TRIG}	Trigger current	V_{TRIG} = 0 V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC} = 15 V, V_{TH} = 10.5 V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current Reset current	V_{RESET} = 0.4 V V_{RESET} = 0 V		0.1 0.4	0.4 1.0		0.1 0.4	0.4 1.5	mA mA
V_{OL}	LOW-level output voltage	V_{CC} = 15 V I_{SINK} = 10 mA I_{SINK} = 50 mA I_{SINK} = 100 mA I_{SINK} = 200 mA		 0.1 0.4 2.0 2.5	 0.15 0.5 2.2 		 0.1 0.4 2.0 2.5	 0.25 0.75 2.5 	 V V V V
		V_{CC} = 5 V I_{SINK} = 8 mA I_{SINK} = 5 mA		 0.1 0.05	 0.25 0.2		 0.3 0.25	 0.4 0.35	 V V
V_{OH}	HIGH-level output voltage	V_{CC} = 15 V I_{SOURCE} = 200 mA I_{SOURCE} = 100 mA	 13.0	 12.5 13.3	 	 12.75	 12.5 13.3	 	 V V
		V_{CC} = 5 V I_{SOURCE} = 100 mA	 3.0	 3.3	 	 2.75	 3.3	 	 V
t_{OFF}	Turn-off time[5]	V_{RESET} = V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:

1. Supply current when output high typically 1 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the max value of R_A+R_B, for 15 V operation, the max total R = 10 MΩ, and for 5 V operation, the max. total R = 3.4 MΩ.
4. Specified with trigger input HIGH.
5. Time measured from a positive-going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from HIGH to LOW of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

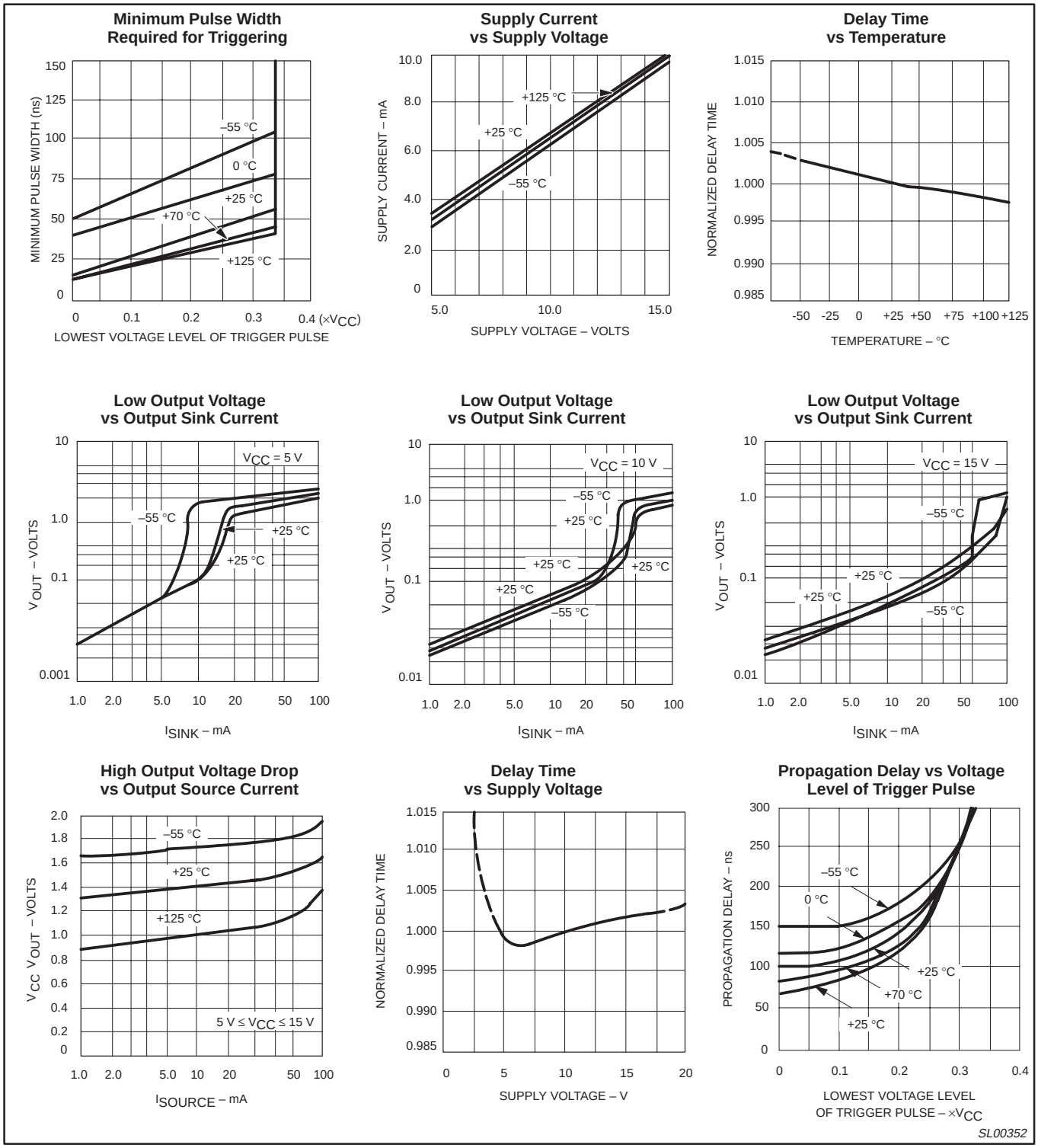
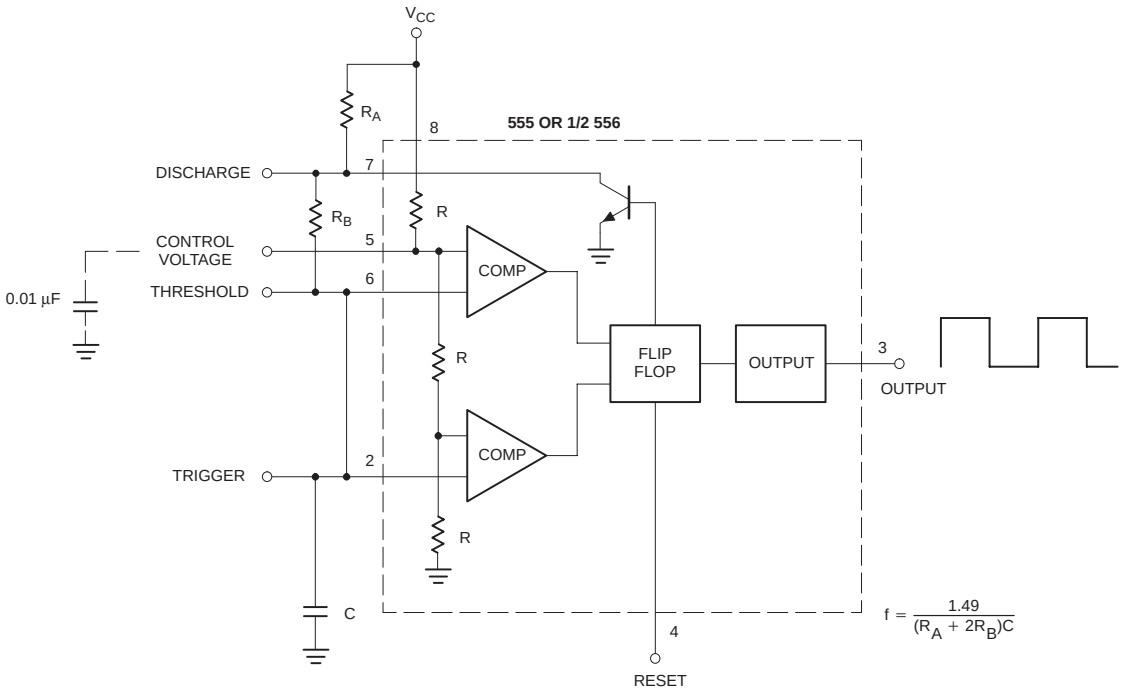
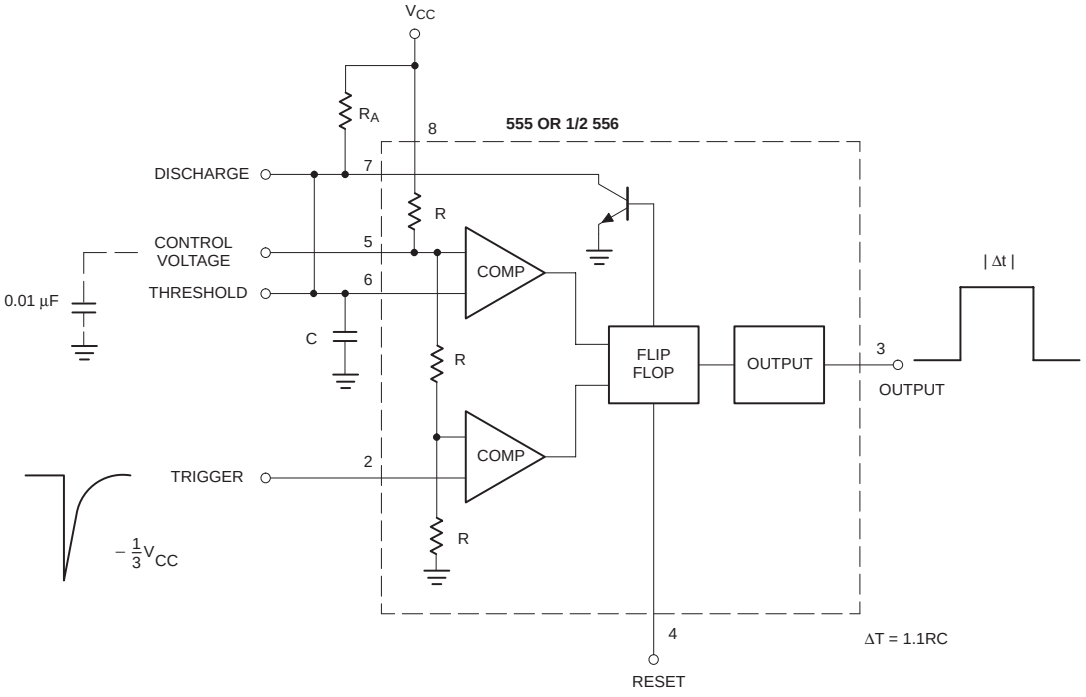


Figure 4. Typical Performance Characteristics

TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

SL00353

Figure 5. Typical Applications

TYPICAL APPLICATIONS

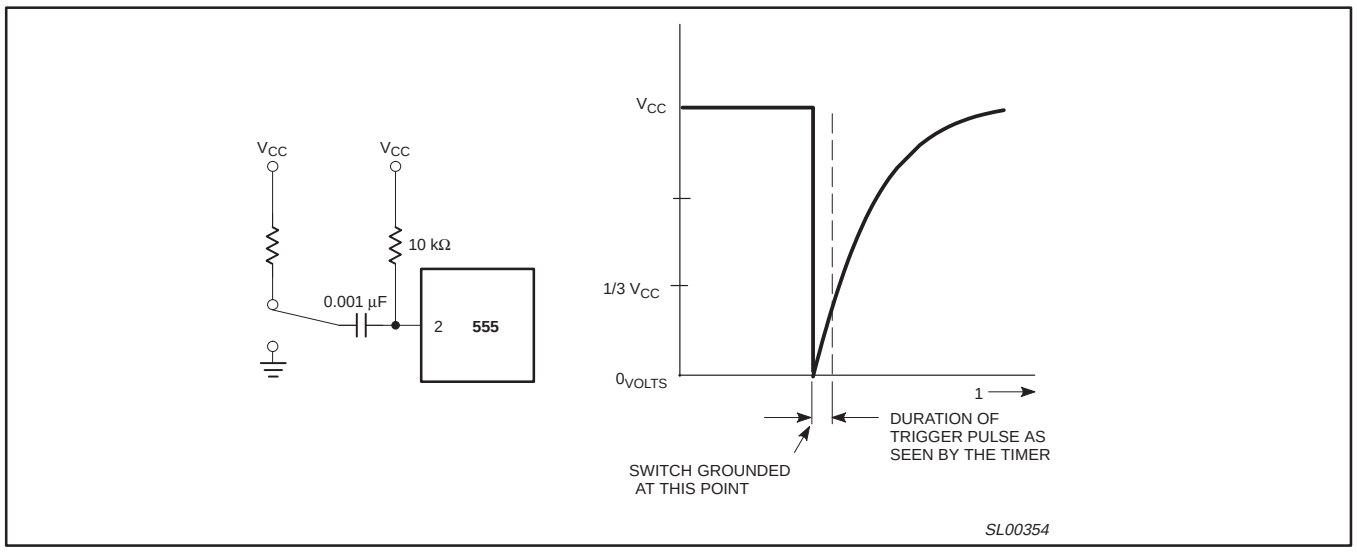


Figure 6. AC Coupling of the Trigger Pulse

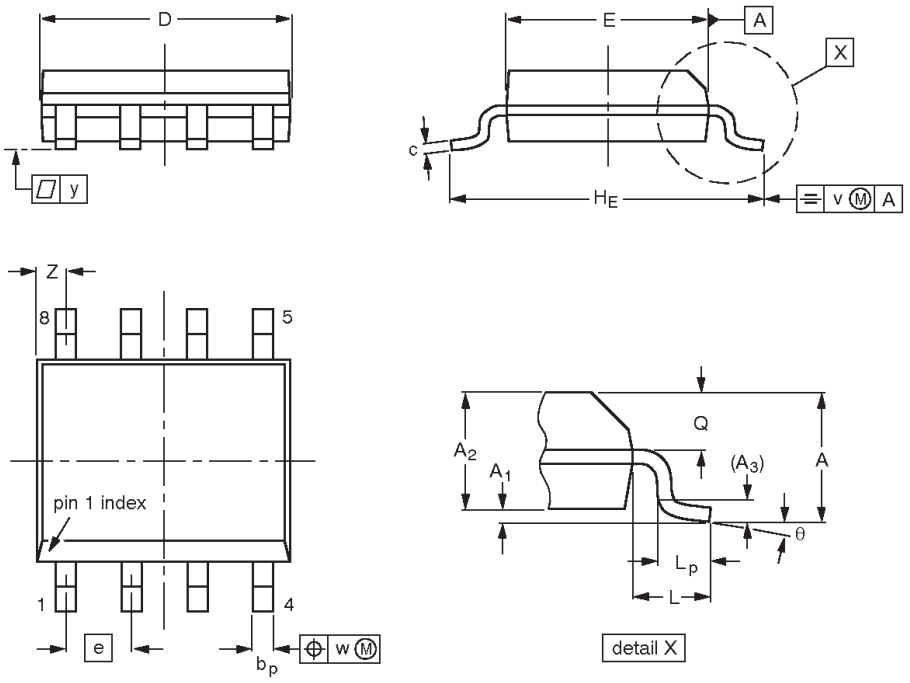
Trigger Pulse Width Requirements and Time Delays

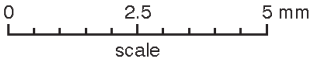
Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 6, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the “turn-off time”. This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2 µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as “turn off time”. This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

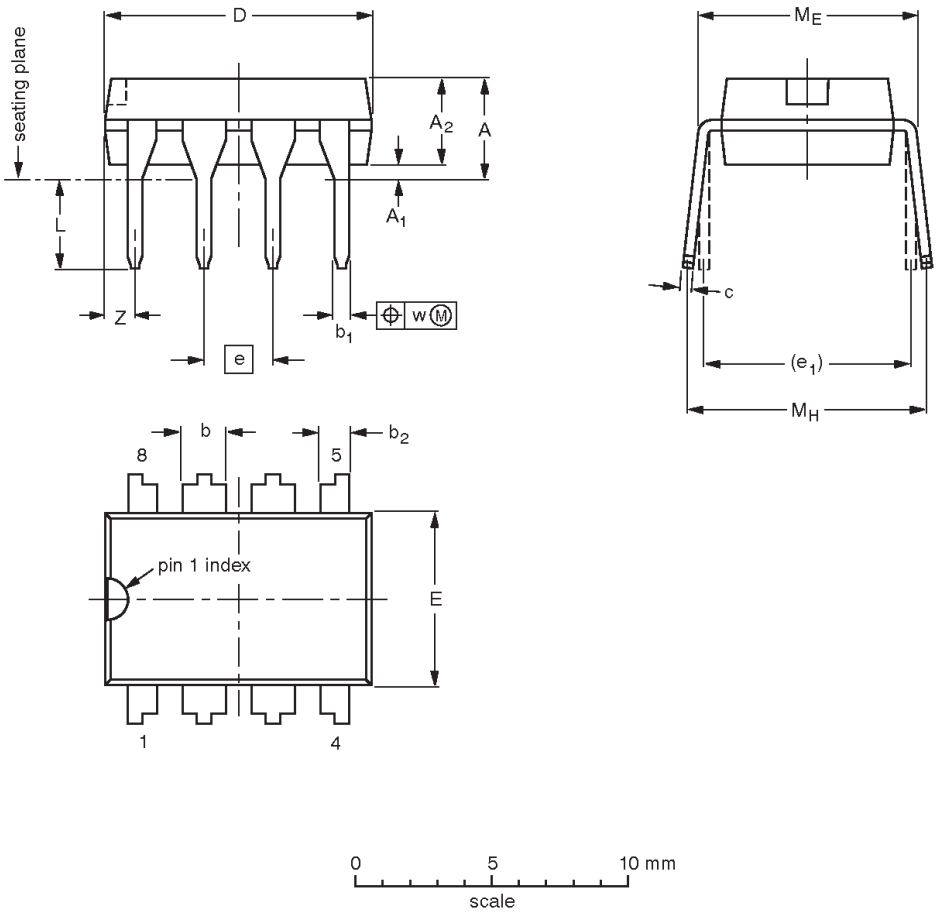
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_2	20030214	**Product data (9397 750 11129); ECN 853-0036 29156 of 06 November 2002. Supersedes Product specification dated August 31, 1994.** Modifications: ● Remove all cerdip information from the data sheet. Package type discontinued. ● 'Absolute maximum ratings' table: T_{SOLD} rating changed from '+300 °C' to '+230 °C'.
	19940831	**Product specification; ECN 853-0036 13721 of 31 August 1994.** (Filename = NE_SA555X.pdf)

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 02-03

Document order number: 9397 750 11129

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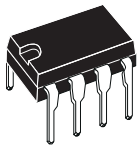
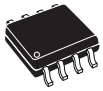
NE555
SA555 - SE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER^{O}C





N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

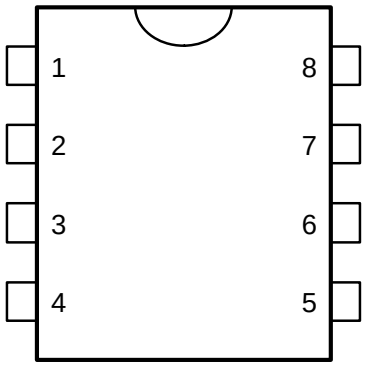
DESCRIPTION

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

ORDER CODES

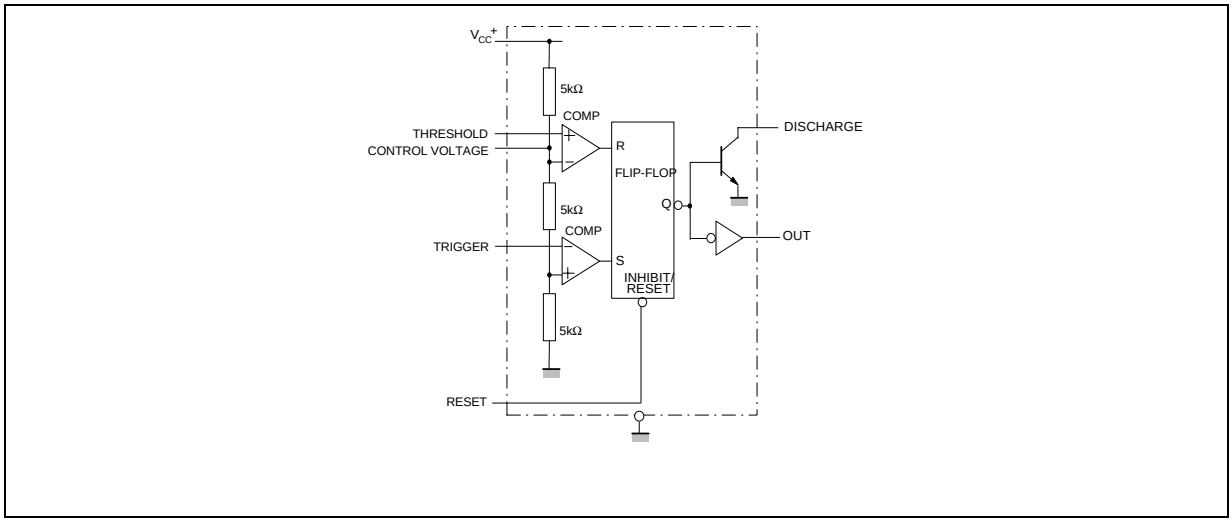
Part Number	Temperature Range	Package	
		N	D
NE555	0^{o}C, 70^{o}C	•	•
SA555	–40^{o}C, 105^{o}C	•	•
SE555	–55^{o}C, 125^{o}C	•	•

PIN CONNECTIONS (top view)

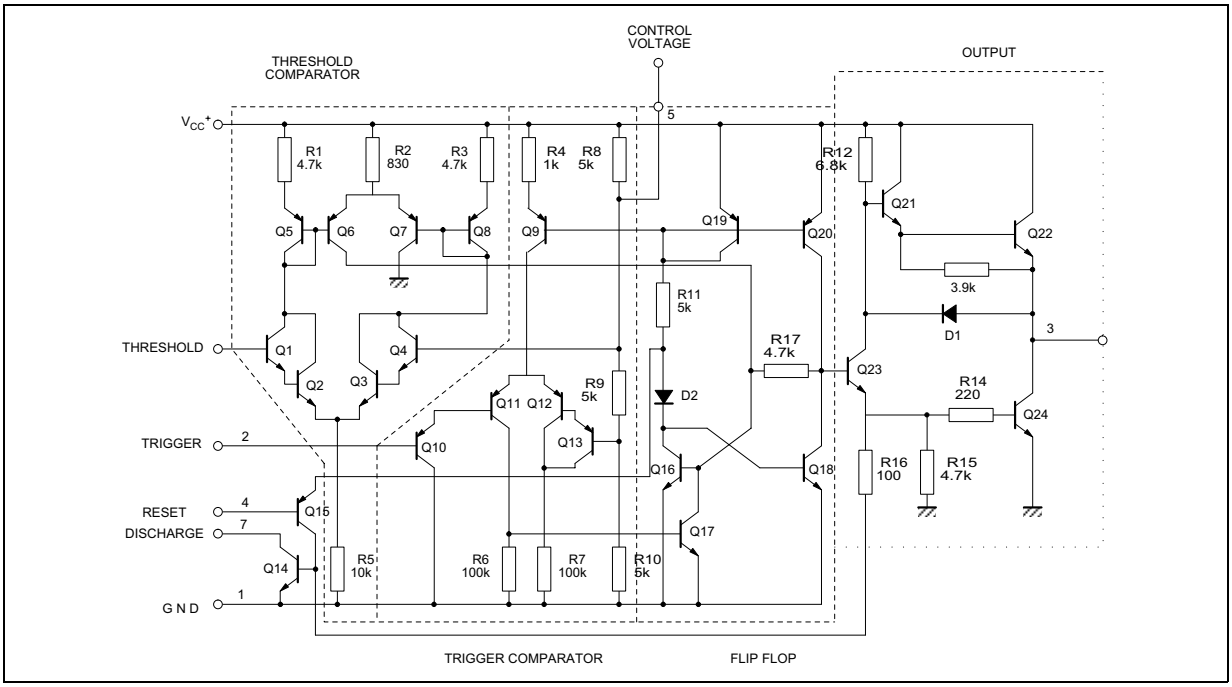


1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{cc}	Supply Voltage		18	V
T_{oper}	Operating Free Air Temperature Range	for NE555 for SA555 for SE555	0 to 70 –40 to 105 –55 to 125	^oC
T_j	Junction Temperature		150	^oC
T_{stg}	Storage Temperature Range		–65 to 150	^oC

OPERATING CONDITIONS

Symbol	Parameter	SE555	NE555 - SA555	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (R_L ∞) (- note 1) Low State V_{CC} = +5V V_{CC} = +15V High State V_{CC} = 5V		 3 10 2	 5 12		 3 10 2	 6 15	mA
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1µF) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 0.5 30 0.05	 2 100 0.2		 1 50 0.1	 3 0.5	 % ppm/°C %/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 1.5 90 0.15			 2.25 150 0.3		 % ppm/°C %/V
V_{CL}	Control Voltage level V_{CC} = +15V V_{CC} = +5V	 9.6 2.9	 10 3.33	 10.4 3.8	 9 2.6	 10 3.33	 11 4	V
V_{th}	Threshold Voltage V_{CC} = +15V V_{CC} = +5V	 9.4 2.7	 10 3.33	 10.6 4	 8.8 2.4	 10 3.33	 11.2 4.2	V
I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage V_{CC} = +15V V_{CC} = +5V	 4.8 1.45	 5 1.67	 5.2 1.9	 4.5 1.1	 5 1.67	 5.6 2.2	V
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current V_{reset} = +0.4V V_{reset} = 0V		 0.1 0.4	 0.4 1		 0.1 0.4	 0.4 1.5	mA
V_{OL}	Low Level Output Voltage V_{CC} = +15V, $I_{O(sink)}$ = 10mA $I_{O(sink)}$ = 50mA $I_{O(sink)}$ = 100mA $I_{O(sink)}$ = 200mA V_{CC} = +5V, $I_{O(sink)}$ = 8mA $I_{O(sink)}$ = 5mA		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	V
V_{OH}	High Level Output Voltage V_{CC} = +15V, $I_{O(source)}$ = 200mA $I_{O(source)}$ = 100mA V_{CC} = +5V, $I_{O(source)}$ = 100mA	 13 3	 12.5 13.3 3.3		 12.75 2.75	 12.5 13.3 3.3		V

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V.
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation the max total R = 3.5MΩ.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering

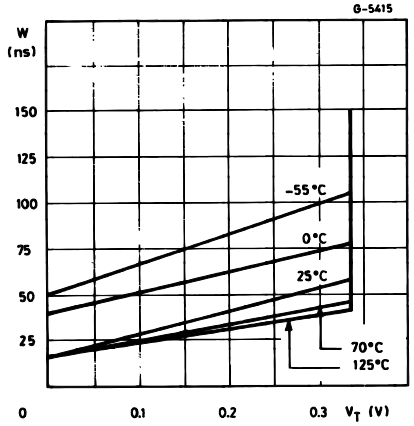


Figure 2 : Supply Current versus Supply Voltage

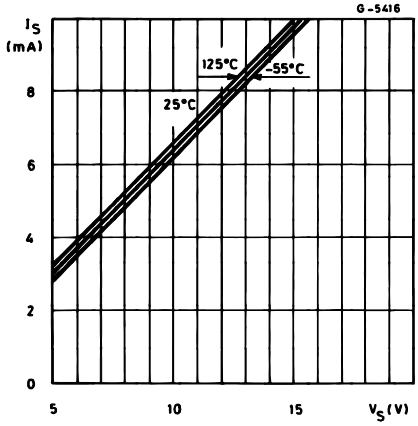


Figure 3 : Delay Time versus Temperature

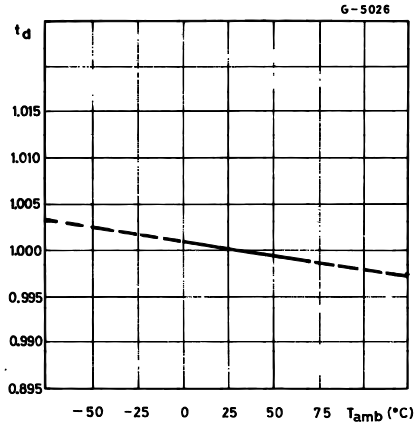


Figure 4 : Low Output Voltage versus Output Sink Current

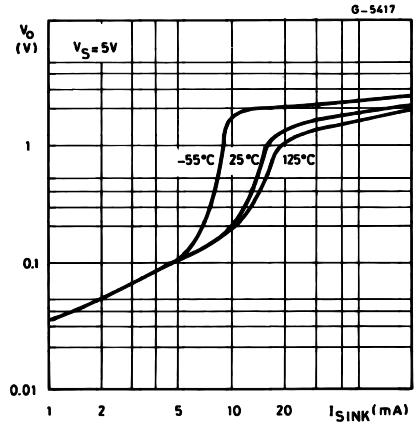


Figure 5 : Low Output Voltage versus Output Sink Current

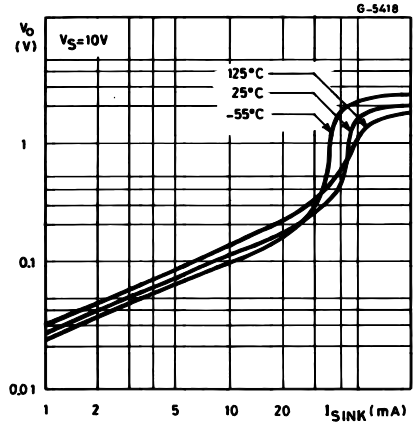


Figure 6 : Low Output Voltage versus Output Sink Current

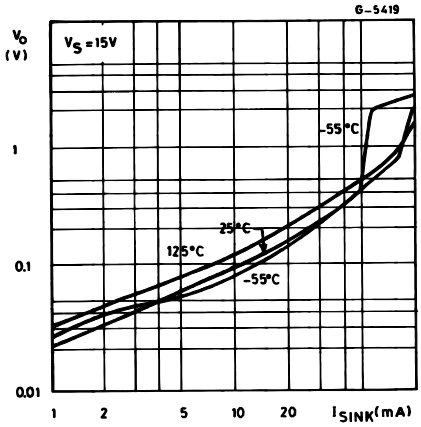


Figure 7 : High Output Voltage Drop versus Output

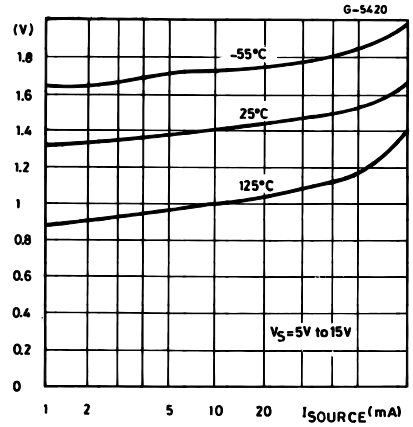


Figure 8 : Delay Time versus Supply Voltage

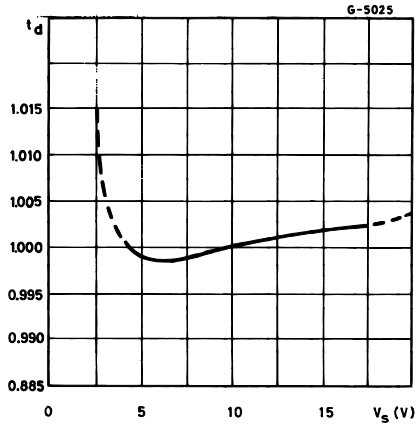
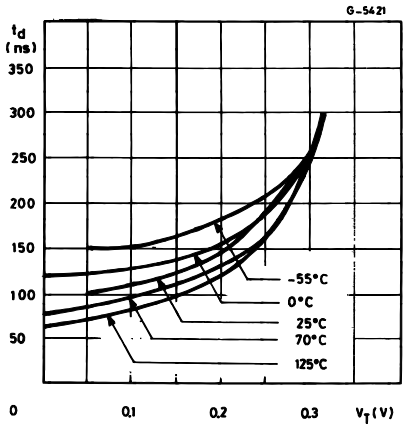


Figure 9 : Propagation Delay versus Voltage Level of Trigger Value

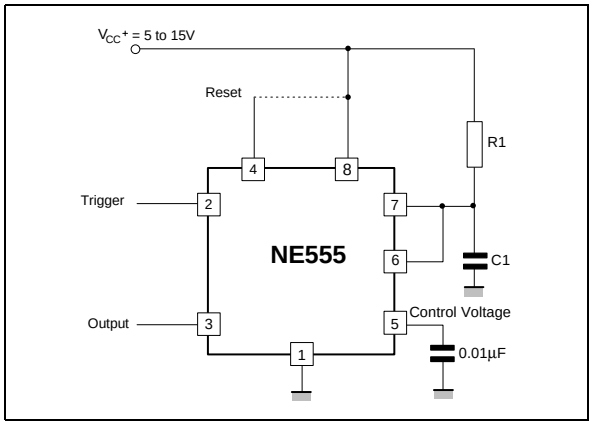


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 10



The circuit triggers on a negative-going input signal when the level reaches 1/3 Vcc. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1C_1$ and is easily determined by figure 12.

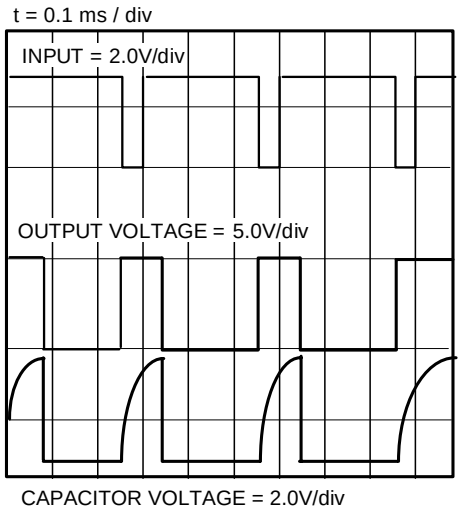
Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1C_1$. When the voltage across the capacitor equals 2/3 V_{cc}, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

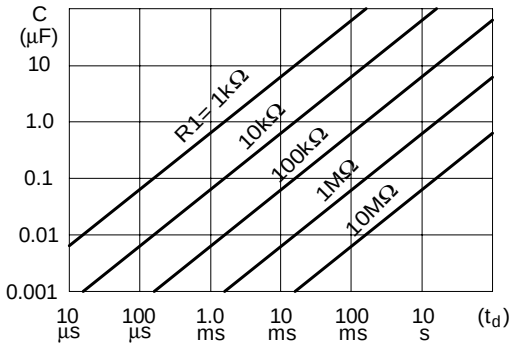
When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11



$R1 = 9.1k\Omega$, $C1 = 0.01\mu F$, $R_L = 1k\Omega$

Figure 12



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{cc} and 2/3 Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 13

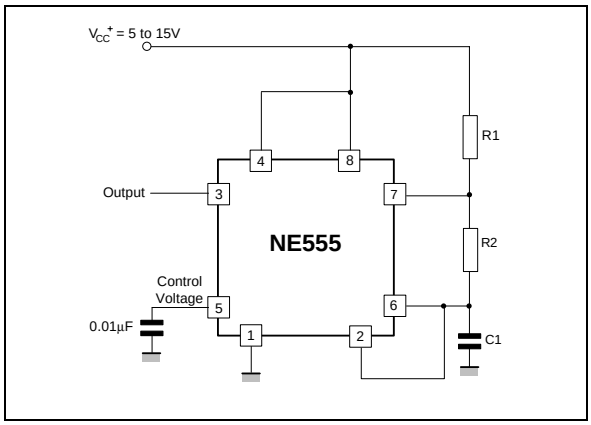


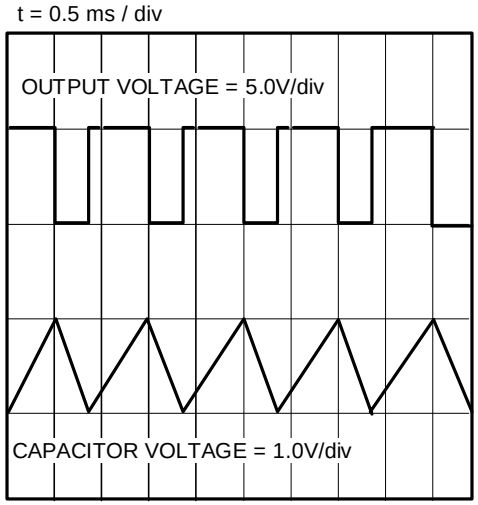
Figure 14 shows actual waveforms generated in this mode of operation.
The charge time (output HIGH) is given by :
$t_1 = 0.693 (R_1 + R_2) C_1$
and the discharge time (output LOW) by :
$t_2 = 0.693 (R_2) C_1$
Thus the total period T is given by :
$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$
The frequency ofoscillation is them :

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)\, C_1}$$

and may be easily found by figure 15.
The duty cycle is given by :

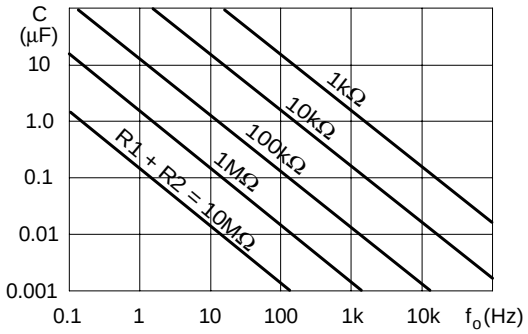
$$D = \frac{R_2}{R_1 + 2R_2}$$

Figure 14



R1 = R2 = 4.8kΩ, C1= 0.1µF, R_L = 1kΩ

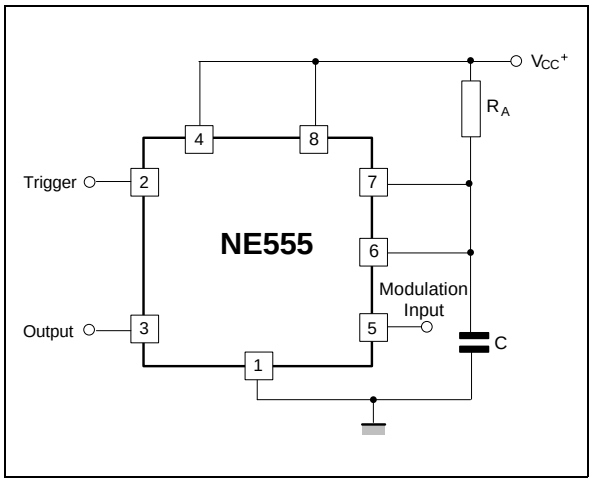
Figure 15 : Free Running Frequency versus R_1, R_2 and C_1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

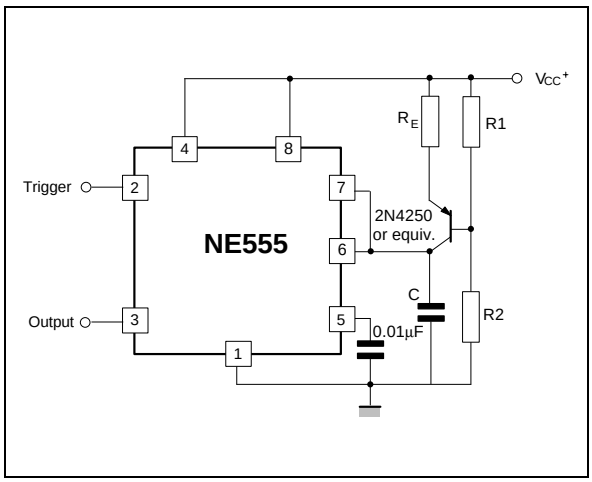
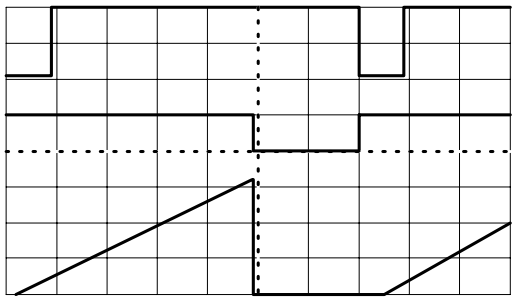


Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_{1+}\ R_{2)})\ C}{R_1\ V_{CC} - V_{BE}\ (R_{1+}\ R_{2)}} \quad V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.



V_{CC} = 5V
Time = 20µs/DIV
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7kΩ
C = 0.01µF

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle the resistors R_A and R_E may be connected as in figure 19. The time preriod for the output high is the same as previous,

$t_1 = 0.693\ R_A\ C$.

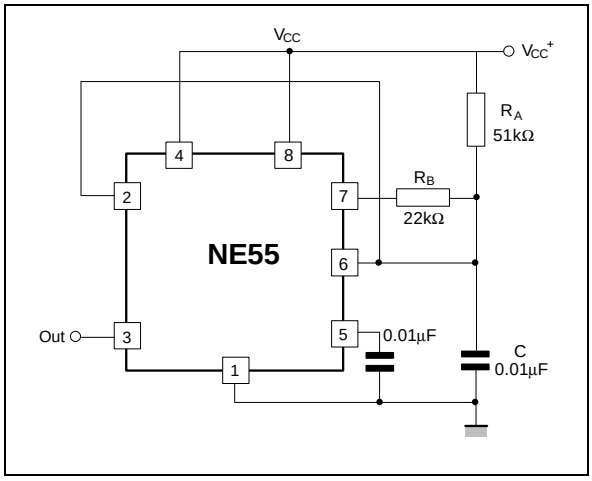
For the output low it is t_2 =

$$[(R_A R_B)/(R_A + R_B)]\ C \mathrm{Ln}\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Note that this circuit will not oscillate if R_B is greater

Figure 19 : 50% Duty Cycle Oscillator.



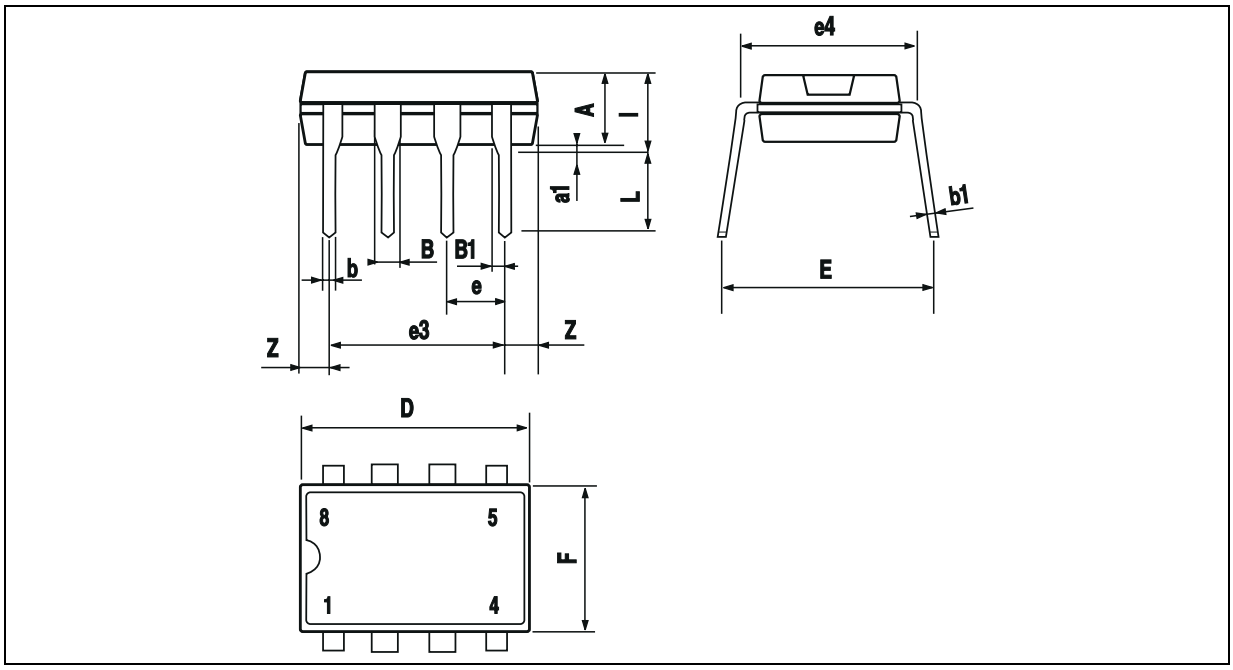
than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



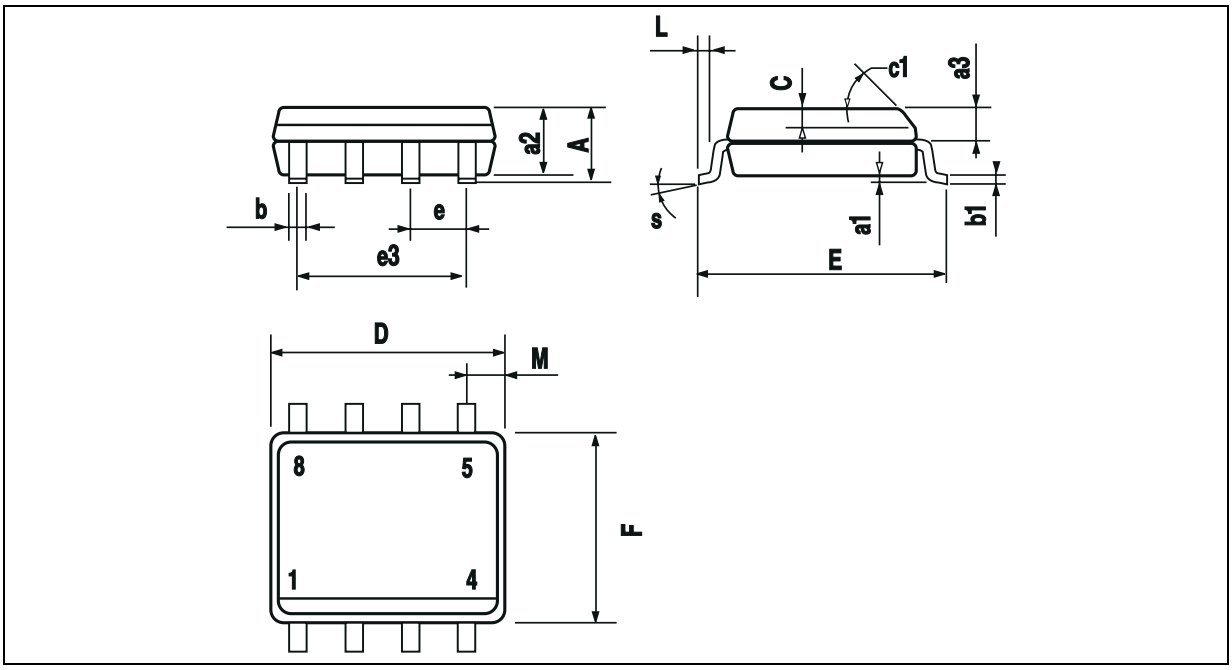
PM-DIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45^o (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8^o (max.)					

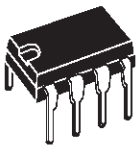
SO8.TBL

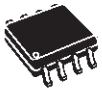
ORDER CODE :

NE555
SA555 - SE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER^{O}C





N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

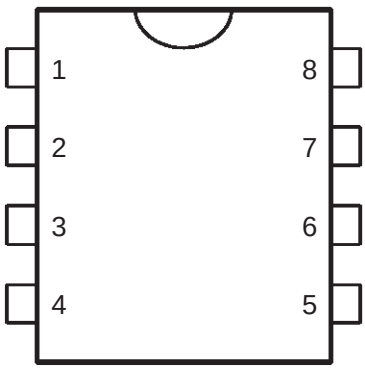
DESCRIPTION

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

ORDER CODES

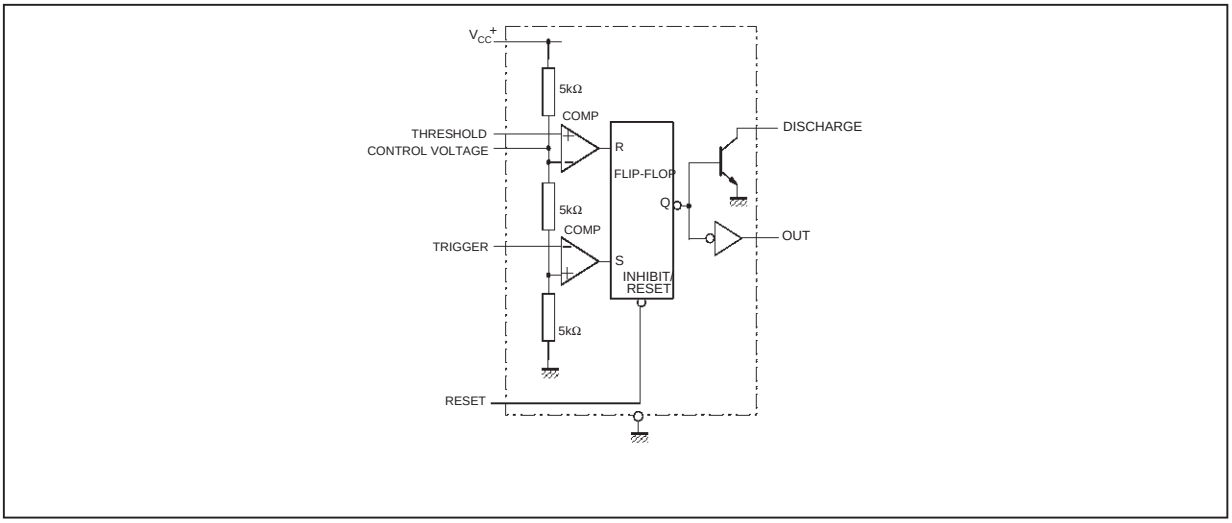
Part Number	Temperature Range	Package	
		N	D
NE555	0^{o}C, 70^{o}C	•	•
SA555	–40^{o}C, 105^{o}C	•	•
SE555	–55^{o}C, 125^{o}C	•	•

PIN CONNECTIONS (top view)

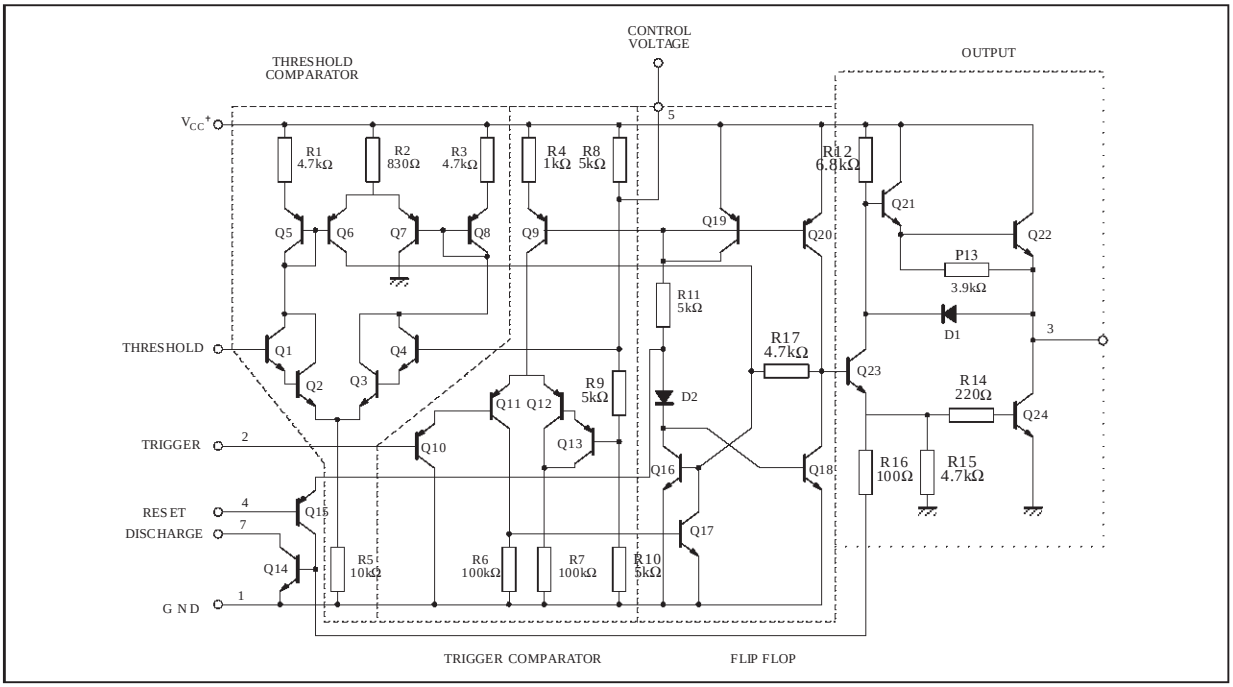


1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{cc}	Supply Voltage	18	V
T_{oper}	Operating Free Air Temperature Range for NE555 for SA555 for SE555	0 to 70 –40 to 105 –55 to 125	°C
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	–65 to 150	°C

OPERATING CONDITIONS

Symbol	Parameter	SE555	NE555 - SA555	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (R_L ∞) (- note 1) Low State V_{CC} = +5V V_{CC} = +15V High State V_{CC} = 5V		 3 10 2	 5 12		 3 10 2	 6 15	mA
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1µF) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 0.5 30 0.05	 2 100 0.2		 1 50 0.1	 3 0.5	 % ppm/°C %/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 1.5 90 0.15	 		 2.25 150 0.3	 	 % ppm/°C %/V
V_{CL}	Control Voltage level V_{CC} = +15V V_{CC} = +5V	 9.6 2.9	 10 3.33	 10.4 3.8	 9 2.6	 10 3.33	 11 4	V
V_{th}	Threshold Voltage V_{CC} = +15V V_{CC} = +5V	 9.4 2.7	 10 3.33	 10.6 4	 8.8 2.4	 10 3.33	 11.2 4.2	V
I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage V_{CC} = +15V V_{CC} = +5V	 4.8 1.45	 5 1.67	 5.2 1.9	 4.5 1.1	 5 1.67	 5.6 2.2	V
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current V_{reset} = +0.4V V_{reset} = 0V	 	 0.1 0.4	 0.4 1	 	 0.1 0.4	 0.4 1.5	mA
V_{OL}	Low Level Output Voltage V_{CC} = +15V, $I_{O(sink)}$ = 10mA $I_{O(sink)}$ = 50mA $I_{O(sink)}$ = 100mA $I_{O(sink)}$ = 200mA V_{CC} = +5V, $I_{O(sink)}$ = 8mA $I_{O(sink)}$ = 5mA		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	V
V_{OH}	High Level Output Voltage V_{CC} = +15V, $I_{O(source)}$ = 200mA $I_{O(source)}$ = 100mA V_{CC} = +5V, $I_{O(source)}$ = 100mA	 13 3	 12.5 13.3 3.3	 	 12.75 2.75	 12.5 13.3 3.3	 	V

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V.
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation the max total R = 3.5MΩ.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering

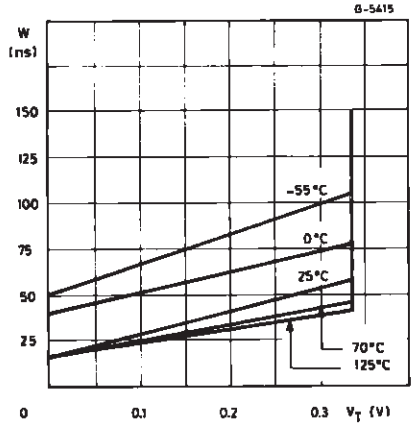


Figure 2 : Supply Current versus Supply Voltage

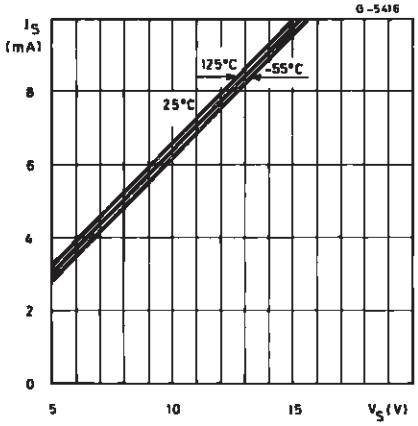


Figure 3 : Delay Time versus Temperature

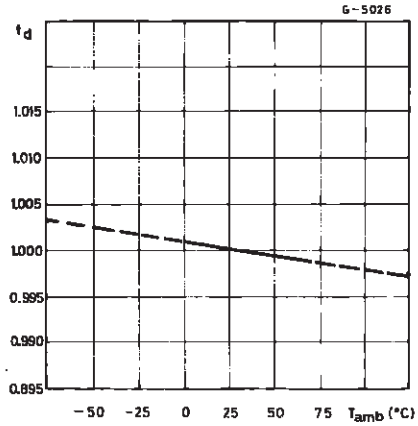


Figure 4 : Low Output Voltage versus Output Sink Current

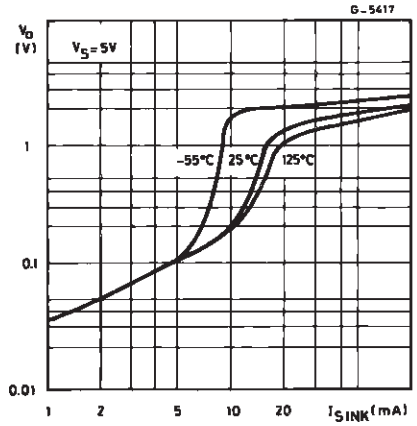


Figure 5 : Low Output Voltage versus Output Sink Current

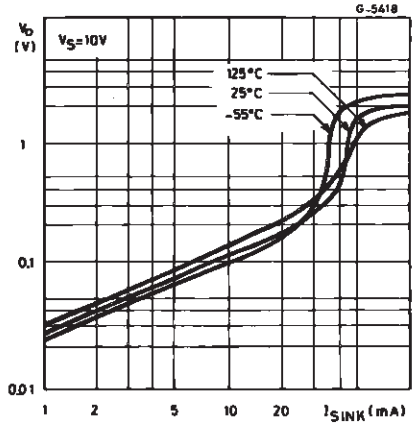


Figure 6 : Low Output Voltage versus Output Sink Current

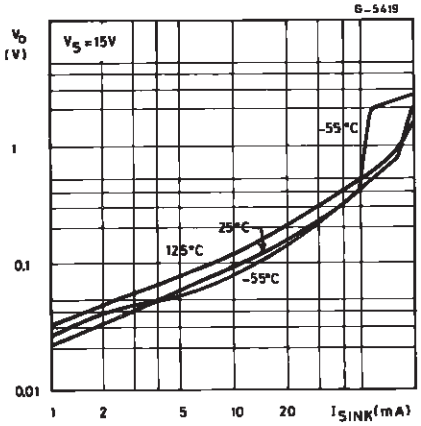


Figure 7 : High Output Voltage Drop versus Output

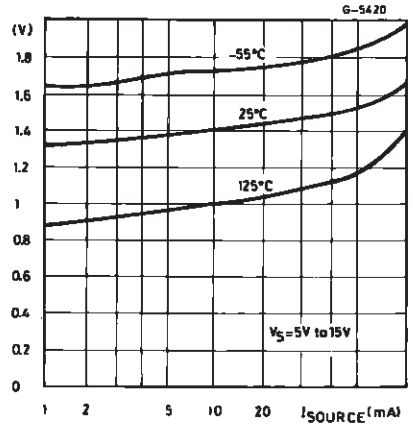


Figure 8 : Delay Time versus Supply Voltage

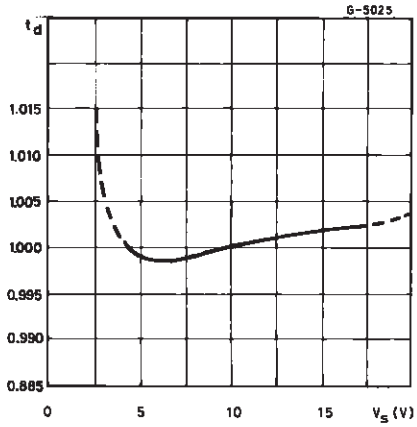
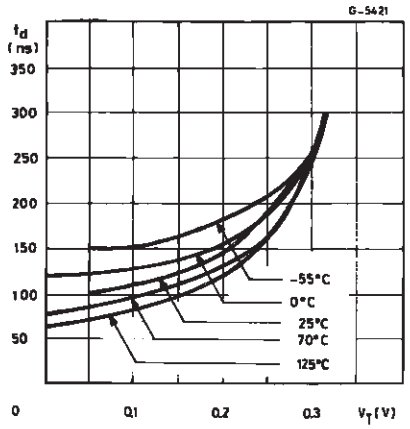


Figure 9 : Propagation Delay versus Voltage Level of Trigger Value

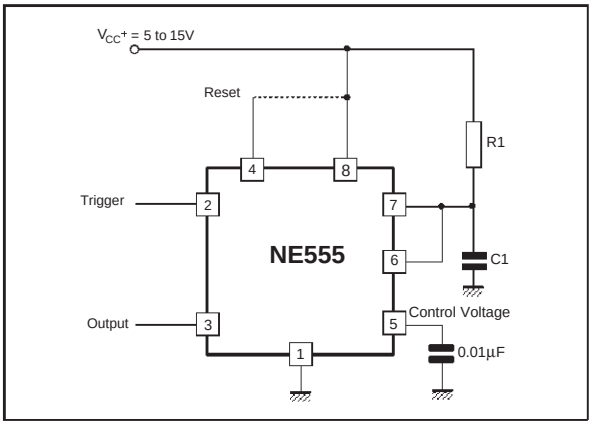


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 10



The circuit triggers on a negative-going input signal when the level reaches 1/3 Vcc. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1C_1$ and is easily determined by figure 12.

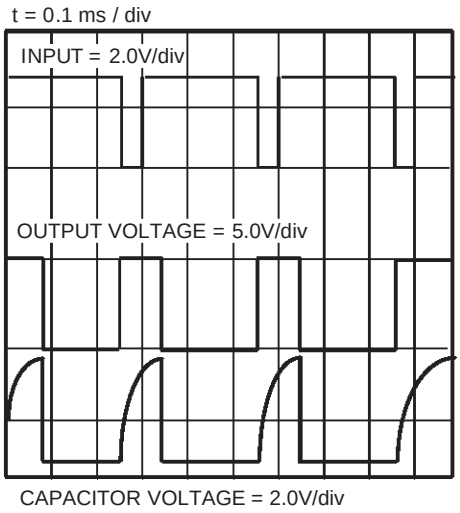
Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1C_1$. When the voltage across the capacitor equals 2/3 V_{cc}, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

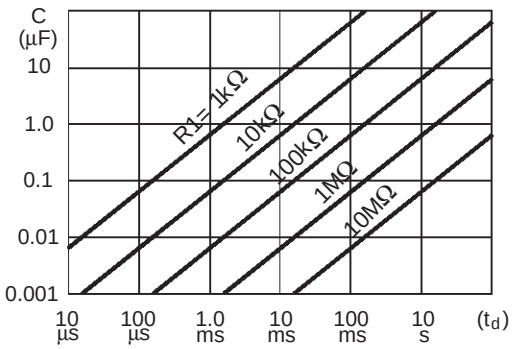
When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11



$R1 = 9.1k\Omega$, $C1 = 0.01\mu F$, $R_L = 1k\Omega$

Figure 12



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{cc} and 2/3 Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 13

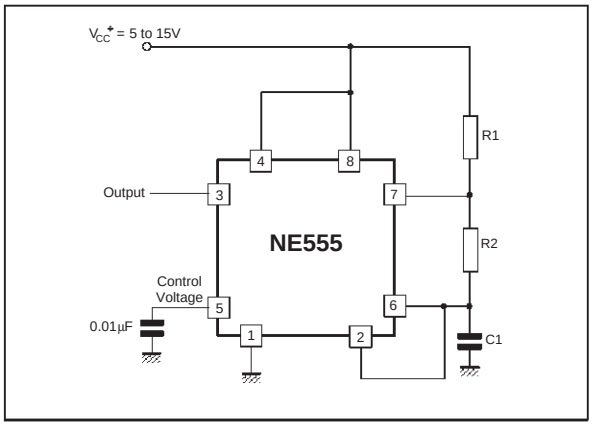


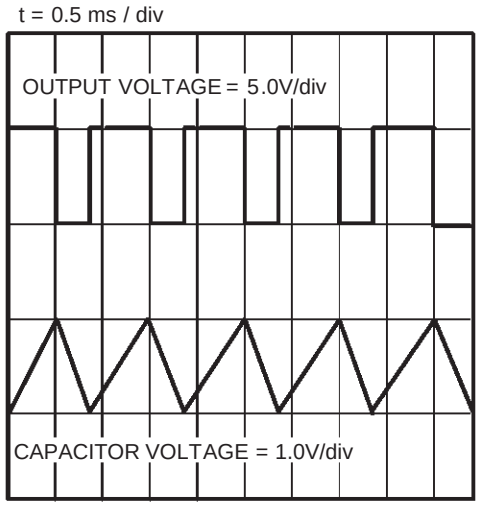
Figure 14 shows actual waveforms generated in this mode of operation.
The charge time (output HIGH) is given by :
$t_1 = 0.693 (R_1 + R_2) C_1$
and the discharge time (output LOW) by :
$t_2 = 0.693 (R_2) C_1$
Thus the total period T is given by :
$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$
The frequency ofoscillation is them :

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)\ C_1}$$

and may be easily found by figure 15.
The duty cycle is given by :

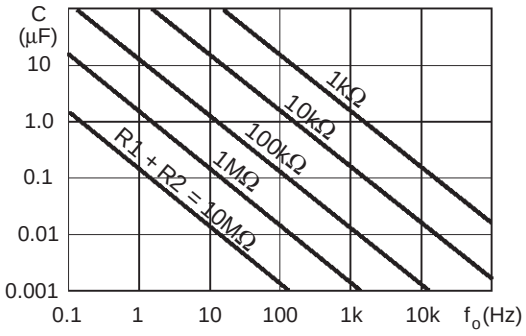
$$D = \frac{R_2}{R_1 + 2R_2}$$

Figure 14



R1 = R2 = 4.8kΩ, C1= 0.1µF, R_L = 1kΩ

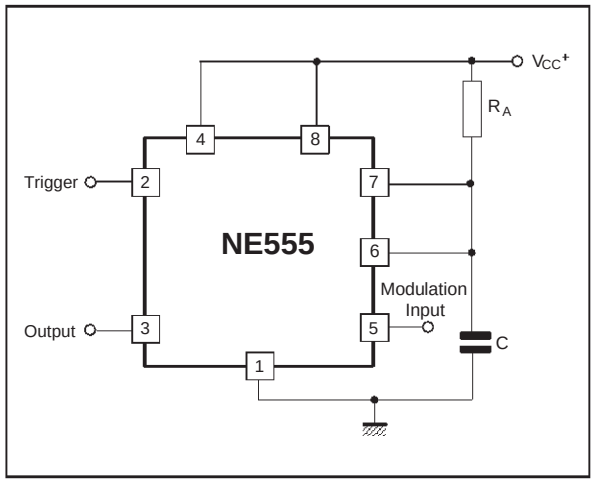
Figure 15 : Free Running Frequency versus R_1, R_2 and C_1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

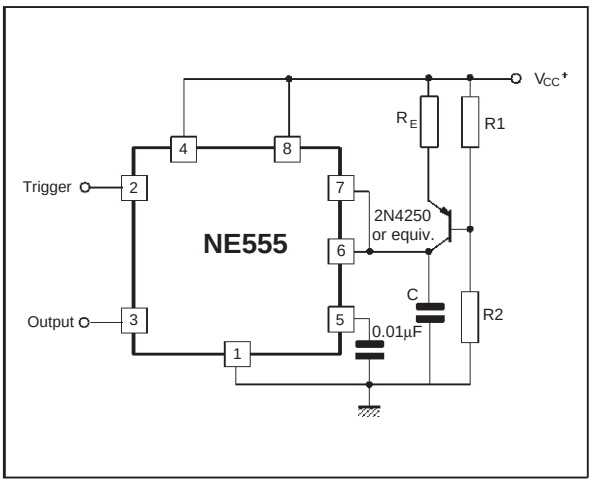
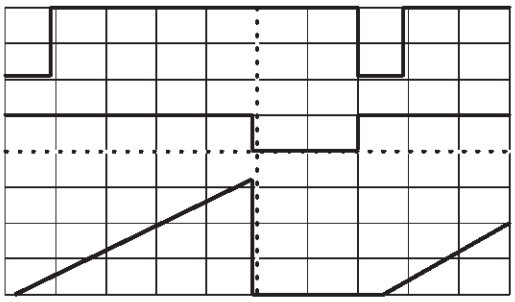


Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_{1+}\ R_{2)}\ C}{R_1\ V_{CC} - V_{BE}\ (R_{1+}\ R_{2)}} \quad V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.



V_{CC} = 5V
Time = 20µs/DIV
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7kΩ
C = 0.01µF

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle the resistors R_A and R_E may be connected as in figure 19. The time preriod for the output high is the same as previous,

$t_1 = 0.693\ R_A\ C.$

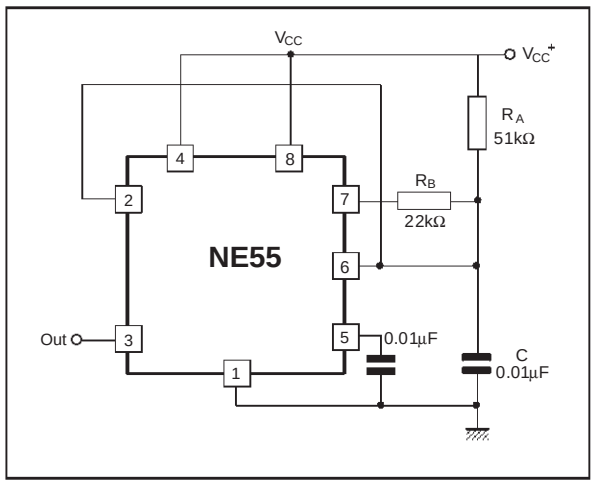
For the output low it is $t_2 =$

$$[(R_A R_B)/(R_A + R_B)]\ CLn\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

Figure 19 : 50% Duty Cycle Oscillator.

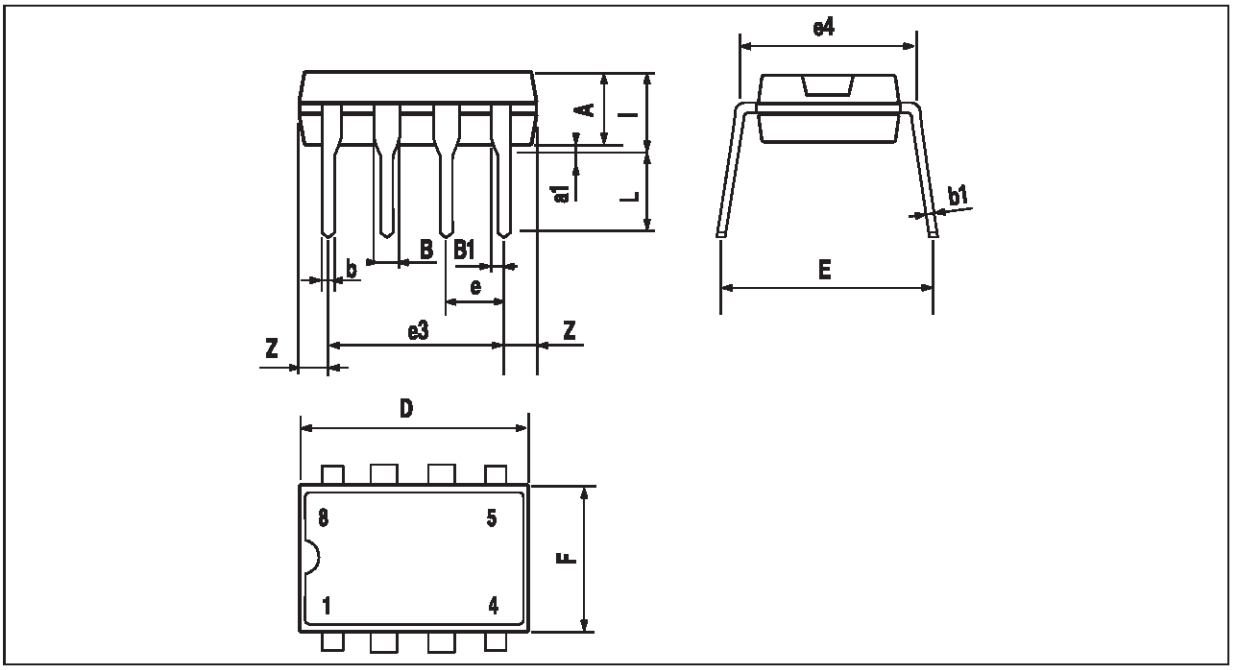


ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



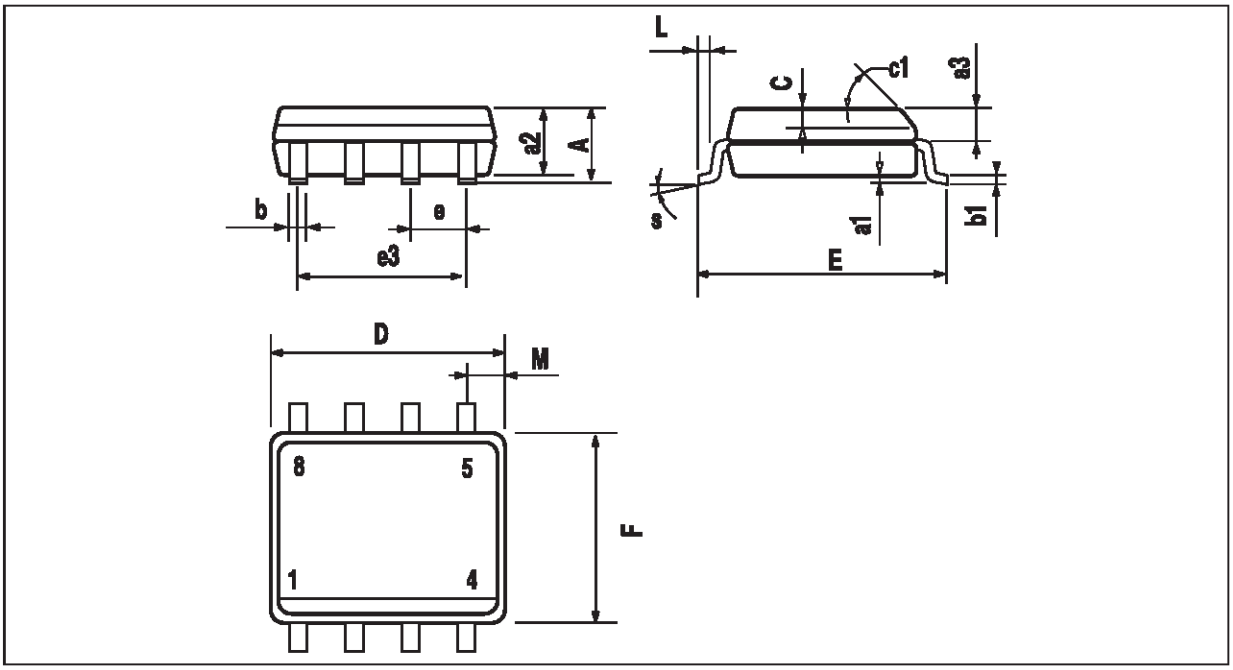
PM-DIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SO8.TBL

ORDER CODE :